STIC Search Report
EIC 2800

STIC Database Tracking Number: 119248

TO: Monica Lewis
Location: JEF 5A30
Art Unit : 2822
Tuesday, April 20, 2004

Case Serial Number: 09/805597

From: Irina Speckhard
Location: EIC 2800 JEF 4B59
Phone: (571) 272-2554
irina.speckhard@uspto.gov

Search Notes

Examiner Lewis,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 4/19/04 Serial # 09/805,597 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2899 Phone 272-1737 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC s archer normally will contact you before beginning a prior art search. If you would like to sit with a s archer for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 04-12-04 A11:14 IN

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-4, 7+8

Problem: See page 1

Solution: " " abstract

US 2002/0096748

US 5,789,803 US 2001/0048116

Staff Use Only

Searcher: Jeff Harrison

Searcher Phone: _____

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 4/20/04

Date Completed: 4/20/04

Searcher Prep/Rev Time: 180

Online Time: 140

Type of Search

Structure (#) _____

Bibliographic ✓

Litigation _____

Fulltext _____

Patent Family _____

Other au, cit's.

Vendors

STN _____

Dialog ✓

Questel/Orbit _____

Lexis-Nexis _____

WWW/Internet _____

Other _____

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact***:

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

20apr04 14:22:58 User267149 Session D1348.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2004/Apr W2
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File 6:NTIS 1964-2004/Apr W3
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*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2004/Mar
(c) 2004 DECHEMA
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200425
(c) 2004 Thomson Derwent
*File 350: For more current information, include File 331 in your search. Enter HELP NEWS 331 for details.
File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
(c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2004/Mar
(c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	2613658	SEMICONDUCT?
S2	47172	(LEADFRAM? OR LEAD()FRAM?)
S3	19580	(MULTIPL? OR MULTI OR MANY OR SEVERAL)(3N)LEAD? ?
S4	65285	S2:S3
S5	5944	(SOURCE? OR GATE?)(3N)ATTACH?
S6	153459	(FIRST OR SECOND OR ONE OR TWO)(3N)SOURCE? ?
S7	5487	ATTACH?(3N)AREA? ?
S8	164456	S5:S7
S9	2315202	DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP OR ETCH???????? OR CUT OR TRIM?
S10	61021	(ATTACH? OR FASTEN? OR AFFIX? OR CONNECT? OR JOIN? OR LINK? OR COUPL? OR STACK??? OR MOUNT? OR PILE OR PILED OR MOUND? OR BUMPED)(3N)(DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP OR ETCH???????? OR CUT OR TRIM?)
S11	2315202	S9:S10
S12	21635	ELECTRICAL?(3N)(COUPLED? OR COUPLING)
S13	37931	DRAIN?(3N)(CONNET? OR REGION? OR CLIP? ?)
S14	3018198	BODY
S15	28091	S1 AND S4
S16	91	S15 AND S8
S17	48	S16 AND S11
S18	3	S17 AND S12
S19	3	RD (unique items)
S20	45	S17 NOT S18
S21	1	S20 AND S13
S22	44	S20 NOT S21
S23	6	S22 AND S14
S24	6	RD (unique items)
S25	38	S22 NOT S23
S26	38	S25 AND S2
S27	3	S26 AND S3
S28	3	RD (unique items)
S29	35	S26 NOT S27
S30	35	RD (unique items)
S31	0	S30 AND S3
S32	35	S30 AND S9
S33	13664	S11 AND S4
S34	13664	S33 AND S9
S35	2595	S34 AND S10
S36	1769	S35 AND S1
S37	1716	S36 AND S2
S38	115	S37 AND S3
S39	1	S38 AND S5
S40	114	S38 NOT S39
S41	1	S40 AND S6
S42	113	S40 NOT S41
S43	0	S42 AND S7
S44	0	S42 AND S13
S45	14	S42 AND S14
S46	14	RD (unique items)
S47	14	S46 NOT S18,S21,S23,S27,S39

19/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015355017
WPI Acc No: 2003-415955/200339
XRAM Acc No: C03-110115
XRPX Acc No: N03-331464
Power **semiconductor** package for power junction field effect transistor, includes **semiconductor die** with drain **coupled** to lower plate, source coupled to **leadframe**, and gate coupled to the **leadframe** via conductive ribbon
Patent Assignee: LOVOLTECH INC (LOVO-N)
Inventor: PLANEY B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6528880	B1	20030304	US 2001892128	A	20010625	200339	B

Priority Applications (No Type Date): US 2001892128 A 20010625
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6528880	B1		12	H01L-023/48	

Abstract (Basic): US 6528880 B1
Abstract (Basic):
NOVELTY - Power **semiconductor** package comprises a **semiconductor die** disposed between upper and lower plates having outside dimensions of S08 **semiconductor** package. The **die** has a drain **electrically coupled** to the lower plate, a source **electrically coupled** to a **leadframe** via upper plate, and a gate **electrically coupled** to the **leadframe** via a conductive ribbon.

DETAILED DESCRIPTION - A power **semiconductor** package comprises a bottom **leadframe** having a bottom plate (105) portion and first terminal(s) extending from the bottom portion, second terminal(s) co-planar with the first terminal, a third terminal, a **semiconductor** power enhancement mode junction field effect transistor (JFET) **die** having a bottom surface defining a drain connection and a top surface on which a first metallized region defining a **source** and a **second** metallized region defining gate (160) are disposed, a copper plate coupled to and spanning in a part of the first metallized region defining the source connection, beam (129) portion(s) to couple the copper plate portion to the second terminal so that the second terminal is **electrically coupled** to the source, and a conductive ribbon (122) coupling the gate to the third terminal. The bottom surface is coupled to the bottom plate of the bottom **leadframe** so that the first terminal (121,125) is **electrically coupled** to the drain.

USE - For power junction field effect transistor.

ADVANTAGE - The invention reduces the resistance and inductance of the current paths through gates devices, e.g. MOSFETs and junction field effect transistor.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of terminal connections.

Bottom plate (105)
Leads (120)
Terminal (121,125)
Conductive ribbon (122)
Plate (126)

Beam (129)
Semiconductor die (130)
Metallized region (135)
Housing (140)
Gate (160)
pp; 12 DwgNo 6/7

19/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014560665
WPI Acc No: 2002-381368/200241
Related WPI Acc No: 1998-541884; 2001-048911; 2002-327564
XRAM Acc No: C02-107548
XRPX Acc No: N02-298386
Semiconductor device for converters, comprises two **semiconductor dies** having opposing surfaces containing respective electrodes, thin conductive **lead frame** having main pad area with pins, and molded housing
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: CHEAH C; DAVIS C; KINZER D M
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020008319	A1	20020124	US 9629483	P	19961024	200241	B
			US 97816829	A	19970318		
			US 98161790	A	19980928		
			US 2000645060	A	20000824		
			US 2001966092	A	20011001		
US 6404050	B2	20020611	US 9629483	P	19961024	200244	
			US 97816829	A	19970318		
			US 98161790	A	19980928		
			US 2000645060	A	20000824		
			US 2001966092	A	20011001		

Priority Applications (No Type Date): US 9629483 P 19961024; US 97816829 A 19970318; US 98161790 A 19980928; US 2000645060 A 20000824; US 2001966092 A 20011001
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020008319	A1		10	H01L-029/00	Provisional application US 9629483
					Cont of application US 97816829
					Cont of application US 98161790
					Cont of application US 2000645060
					Cont of patent US 5814884
					Cont of patent US 6133632
					Cont of patent US 6297552
US 6404050	B2			H01L-023/48	Provisional application US 9629483
					Cont of application US 97816829
					Cont of application US 98161790
					Cont of application US 2000645060
					Cont of patent US 5814884
					Cont of patent US 6133632
					Cont of patent US 6297552

Abstract (Basic): US 20020008319 A1
Abstract (Basic):

NOVELTY - **Semiconductor** device comprises two **semiconductor dies**, each with opposing surfaces that contain respective electrodes; and a thin conductive **lead frame** having a main pad area with first pins extending from one edge and second pins separated from one another and from the main pad area. A molded housing encapsulates the **lead frame**, the **dies** and bonding wires.

DETAILED DESCRIPTION - A **semiconductor** device comprises two **semiconductor dies**, each having opposing surfaces that contain respective electrodes; and a thin conductive **lead frame** (40) having a main pad area (41) with first pins (1-4) extending from one edge and second pins (5-8) separated from one another and from the main pad area. The second pins are disposed on an edge of the main pad area opposite to the side containing the first pins. One of the opposing surfaces of each **die** is disposed atop and in electrical contact with the main pad area and laterally spaced from one another. The other opposing surfaces are wire bonded to the respective second pins. A molded housing (30) is provided for encapsulating the **lead frame**, the **dies**, and the bonding wires (50-53). The first and second pins extend beyond the boundary of the molded housing and are available for external connection. INDEPENDENT CLAIMS are also included for:

(a) a converter circuit comprising the **semiconductor** device, a supply voltage terminal coupled to **source** terminal of **first semiconductor die**, a ground terminal **electrically coupled** to anode of second **semiconductor die**, and a pair of load terminals coupled to drain terminal of first **semiconductor die** and to cathode of second **semiconductor die**; and

(b) a synchronous regulator circuit comprising the **semiconductor** device, a supply voltage terminal, a second metal oxide **semiconductor** field effect transistor (MOSFET), a controller coupled to gate terminal of two MOSFETs, and ground terminal **electrically coupled** to source terminal and anode.

USE - As **semiconductor** device for converters.

ADVANTAGE - The **semiconductor** device provides savings in board space while reducing component count and assembly cost. It improves the efficiency of converters by reducing power drain on batteries, thus leading to a longer life. It reduces power dissipation and heat generation near temperature-sensitive parts, e.g., microprocessors.

DESCRIPTION OF DRAWING(S) - The drawing shows a top view of the **lead frame**.

first pins (1-4)
second pins (5-8)
MOSFET **die** (10)
Schottky diode **die** (12)
molded housing (30)
lead frame (40)
main pad area (41)
bonding wires (50-53)
pp; 10 DwgNo 5/9

19/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009764306
WPI Acc No: 1994-044157/199406

XRPX Acc No: N94-035005

Semiconductor package **lead frame** - has protrusions on **die attach area** surface onto which **die** is physically **mounted**

Patent Assignee: MOTOROLA INC (MOTI)

Inventor: BAILEY K W

Number of Countries: 004 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 582084	A2	19940209	EP 93110503	A	19930701	199406	B
EP 582084	A3	19940727	EP 93110503	A	19930701	199529	
JP 7307350	A	19951121	JP 93212091	A	19930805	199604	

Priority Applications (No Type Date): US 92925143 A 19920806

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 582084	A2	E	6	H01L-023/495	
Designated States (Regional): DE FR GB					
JP 7307350	A		5	H01L-021/52	
EP 582084	A3			H01L-023/495	

Abstract (Basic): EP 582084 A

The package **lead frame** includes leads and a **die attach area** (30) with at least one protrusion (34). A **semiconductor die** is **attached** to the **die attach area**, on the protrusion, and **electrically coupled** to the leads. There is an encapsulant about the **die** and part of the **lead frame**.

Pref. there is a dam wall around the **die attach area**. The protrusion may have a flat or radial surface to which the **die** is **attached**. The protrusion height is pref. less than 100mum. In a **die attach** process, the molten **die attach** material flows along protrusions to create a channel effect beneath the **die**.

ADVANTAGE - Enhanced solder wetting to **die attach area** and **die** surface; reduced stress on **die** with even **mounting** and uniform **die attach** material layer.

Dwg.1/2

21/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014929459
WPI Acc No: 2002-750168/200281
XRPX Acc No: N02-590837
Dual **stacked die** package uses two **dice** which are **coupled** to source and **gate attach areas** on surfaces of **lead frame**, where **drain region** of one of **dice** is exposed by packaging material
Patent Assignee: ESTACIO M C B (ESTA-I)
Inventor: ESTACIO M C B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020125550	A1	20020912	US 2001805597	A	20010312	200281	B

Priority Applications (No Type Date): US 2001805597 A 20010312
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020125550	A1		4	H01L-023/495	

Abstract (Basic): US 20020125550 A1
Abstract (Basic):
NOVELTY - The **bumped dice** (30,32) are **coupled** to **source** and gate **attach areas** (20,22,24,25) on respective surfaces of the **lead frame**. A drain connection assembly comprising a **drain clip** (52) and a lead rail, is coupled to the **drain region** of one of the **dice**. A package material surrounds the **dice**, such that the **drain region** of other **die** is exposed.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for dual **stacked die** package manufacturing method.
USE - Dual **stacked die** package.
ADVANTAGE - Parallel connection of chips doubles the silicon performance of the largest chip accommodated in **semiconductor** package, while maintaining existing package layouts. The very low package resistance and thermal performance of the package are maintained reliably.
DESCRIPTION OF DRAWING(S) - The figure shows an exploded view of a **semiconductor** device.
Source attach areas (20,22)
Gate attach areas (24,25)
Bumped dice (30,32)
Drain clip (52)
pp; 4 DwgNo 3/3

24/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014516824
WPI Acc No: 2002-337527/200237
XRAM Acc No: C02-097090
XRPX Acc No: N02-265190
Semiconductor package with **lead frame** having concave portion the flowing speed of the resin mold compound is reduced
Patent Assignee: SILICONWARE PRECISION IND CO LTD (SILI-N)
Inventor: HUANG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 445606	A	20010711	TW 2000103747	A	20000303	200237	B

Priority Applications (No Type Date): TW 2000103747 A 20000303
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 445606	A		16	H01L-023/28	

Abstract (Basic): TW 445606 A
Abstract (Basic):
NOVELTY - A **semiconductor** package with **lead frame** having concave portion, which comprises a **lead frame**, a **die** glued to the **lead frame** and electrically **connected** to the **die** through a plurality of leads, an encapsulating **body** to partly wrap the **lead frame** and form an opening slot to expose the **die** and leads, and a covering piece to seal and cover the encapsulating **body**. The **lead frame** has a **die attach area** for gluing the **die**, and the lead soldering region for electrically connecting to the lead of the **die**, wherein there is at least a concave portion of the **lead frame** formed on the junction portion of the lead soldering region and the encapsulating **body**, and form a concave portion on the junction portion of the lead soldering region and the encapsulating **body**, so that the rate to absorb the heat of packaging mold will be increased since the flowing channel is shallowed after the resin mold compound to form the encapsulating **body** flows into the concave portion during mold pressing.

The absorption of heat of resin mold compound will make it more sticky, thereby the flowing speed of the resin mold compound is reduced, so that the resin mold compound won't flash to the lead soldering region and **die** gluing region, therefore, the contamination of lead soldering region and **die** gluing region can be prevented and the cleaning of flashing can be avoided after the mold pressing is finished, so the packaging process is simplified, the manufacturing cost is reduced, and the quality of **die** gluing and lead soldering is enhanced.

pp; 16 DwgNo 1/7

24/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014469987
WPI Acc No: 2002-290690/200233
XRPX Acc No: N02-226887

Manufacturing method of **semiconductor** package of encapsulating **body** with opening slot - to resolve the problem of flashing

Patent Assignee: SILICONWARE PRECISION IND CO LTD (SILI-N)
Inventor: HUANG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 445605	A	20010711	TW 2000103746	A	20000303	200233	B

Priority Applications (No Type Date): TW 2000103746 A 20000303
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 445605	A			H01L-023/28	

Abstract (Basic): TW 445605 A
Abstract (Basic):

NOVELTY - A manufacturing method of **semiconductor** package, which comprises the following steps: provide a **lead frame** having **die attach area** and lead soldering region; glue a plastic piece made of high-temperature-resistive material to the **lead frame** to cover the **die attach area** and lead soldering region completely; proceed mold pressing to form an encapsulating **body** partly wrapping the **lead frame**, and form an opening slot of the encapsulating **body** on the portion corresponding to the plastic piece for the plastic piece to be exposed to the opening slot; tear off the plastic piece from the **lead frame** to expose the **die attach area** and the lead soldering region; put the **die** on the **die**-loading region and electrically **connect** the **die** to the lead soldering region of the **lead frame**; seal and cover the opening slot of the encapsulating **body** with a covering member air-tightly.

DwgNo 1/1

24/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013605531
WPI Acc No: 2001-089739/200110
XRPX Acc No: N01-067900
Internal heat sink for **semiconductor** package has opening formed in **die** pad, and base pad exposed to encapsulant

Patent Assignee: SILICONWARE PRECISION IND CO LTD (SILI-N)
Inventor: HUANG J; LAI J; RAU R; HUANG C; JAO R; LAI C
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6114752	A	20000905	US 99382742	A	19990825	200110	B
TW 393744	A	20000611	TW 98118651	A	19981110	200112	

Priority Applications (No Type Date): TW 98118651 A 19981110
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6114752	A		12	H01L-023/495	
TW 393744	A			H01L-023/28	

Abstract (Basic): US 6114752 A
Abstract (Basic):

NOVELTY - **Lead frame** (4) has **semiconductor** chip (5) **mounted** on **die** pad (43). Leads (41) extend radially from the **die** pad, which has opening (430) formed to decrease **attaching area**. Base pad (45) is secured by connecting bars (454, 455) directly underneath the **die** pad opening, leaving one surface of the base pad exposed to the resin encapsulant (9). Heat is transferred from **die** pad to base pad, then dissipated to the surroundings.

USE - Dissipation of heat from **semiconductor** package.

ADVANTAGE - Directly dissipates heat through lead **body**. Reduced risk of declamination of the **semiconductor** chip from **die** pad due to thermal stress. Avoids popcorn cracking of the **semiconductor body** during high temperature curing of the package **body**. Prevents moisture from accumulating on the surface of the package. Can be assembled using conventional methods and equipment.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of the **semiconductor body**.

Lead Frame (4)
Semiconductor chip (5)
Resin Encapsulant (9)
Leads (41)
Die pad (43)
Base pad (45)
Opening (430)
Coupling bars (454,455)
pp; 12 DwgNo 3/7

24/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03257457
LEAD FRAME OF RESIN SEALED TYPE **SEMICONDUCTOR** DEVICE

PUB. NO.: 02-232957 [JP 2232957 A]
PUBLISHED: September 14, 1990 (19900914)
INVENTOR(s): MORIMURA MASAHIRO
APPLICANT(s): YAMADA SEISAKUSHO KK [468660] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-053230 [JP 8953230]
FILED: March 06, 1989 (19890306)
JOURNAL: Section: E, Section No. 1008, Vol. 14, No. 546, Pg. 73, December 04, 1990 (19901204)

ABSTRACT

PURPOSE: To thoroughly remove a runner and a gate remaining on a resin main **body** by a method wherein a plating film small in adhesion power to resin is formed on the part of a **lead frame** corresponding to a resin injection path.

CONSTITUTION: A **semiconductor** element (not shown in a figure) is **mounted** on a **die** pad 12 of a **lead frame** 10, the **semiconductor** element is connected to the tips of inner leads 18 through wire bonding, and the **semiconductor** element and the leads 18 are sealed up with resin through a usual method. As a resin injection path is formed at the parting faces of a cope and a drag of a molding **die**, a runner 30 and a gate 32 are left on a side rail 16 of the **lead frame** 10. Then, a plating film A small in adhesion power to resin is

formed on the part of the side rail 16 where the runner 30 and the **gate** 32 are **attached** . Therefore, when the runner 30 and the gate 32 are removed by bending them in a direction that they are separated from the face of the frame 10, they are prevented from remaining attached to the surface of the frame 10.

24/3,AB/5 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03071215
MANUFACTURE OF SOLID ELECTROLYTIC CAPACITOR

PUB. NO.: 02-046715 [JP 2046715 A]
PUBLISHED: February 16, 1990 (19900216)
INVENTOR(s): MIYASHITA TOSHIYUKI
NOMURA HARUO
MITSUI KOICHI
APPLICANT(s): NICHIKON SPRAGUE KK [486107] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-198428 [JP 88198428]
FILED: August 09, 1988 (19880809)
JOURNAL: Section: E, Section No. 922, Vol. 14, No. 210, Pg. 92, April 27, 1990 (19900427)

ABSTRACT

PURPOSE: To facilitate the control of a connection temperature, to lessen a thermal effect to an element and to make small the configuration of the point and the **area** of an electrode **attached** by a pulse heated soldering by a method wherein a fuse is cross-linked and arranged between a cathode layer and a cathode **lead frame** and the fuse and the cathode **lead frame** are connected to each other by pulse heated soldering.

CONSTITUTION: A conductive material containing a solderable metal is applied and formed on a capacitor element 1 made by forming in order a metal oxide substance layer, a **semiconductor** layer and a cathode layer 2 on an anode **body**, which is provided with an anode lead-wire 3 and has a dielectric oxide film on its surface, as a cathode layer of the element 1 and thereafter, an insulating layer 10 is formed on the bottom of the element 1 in such a way as to cover the edge part of the bottom. A **lead frame** formed by **etching** a thin metal plate or by performing a press punching on the thin metal plate is prepared in advance, the layer 2 of the element 1 and a cathode **lead frame** 4 of the **lead frame** are arranged at a distance, a tabular fuse 5 and the frame 4 are arranged on the layer 2 in such a way that the distance part is cross-linked, the fuse 5 and the frame 4 are attached 7 to each other by a pulse heated soldering and after that, at least one surface of the fuse 5 is covered with a resin 6 and a sheathing covering 8 is performed.

24/3,AB/6 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

01487148
MULTI CHIP **SEMICONDUCTOR** DEVICE

PUB. NO.: 59-198748 [JP 59198748 A]

PUBLISHED: November 10, 1984 (19841110)
INVENTOR(s): OWADA ATSUSHI
NAGAE SABURO
APPLICANT(s): NIPPON PRECISION SAAKITSUTSU KK [470120] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-073144 [JP 8373144]
FILED: April 26, 1983 (19830426)
JOURNAL: Section: E, Section No. 303, Vol. 09, No. 61, Pg. 31, March 19, 1985 (19850319)

ABSTRACT

PURPOSE: To improve the space factor, etc. and contrive to suffice **two** power **sources** by internal connection by a method wherein the **semiconductor** substrates of a plurality of **semiconductor** chips whose polarities of operating voltage are different are insulated from each other and thus molded in an integral **body**.

CONSTITUTION: The **semiconductor** chip 4 of a bi-polar type ECL circuit and that 5 of a C-MOS type PLL circuit are adhered on mounting parts 2 and 3 of a **lead frame** 1 formed by punching out a metallic plate, respectively, thus performing wire bonding between each of the **semiconductor** chips 4 and 5 and wire bonding from each electrode to the corresponding lead part 6. At this time, the mounting part 2 is connected to VSS of the **semiconductor** chip 5 in order to connect the **semiconductor** substrate of said chip 4 to VSS of said chip 5. While, VCC of said chip 4 is connected to the mounting part 3 in order to connect VCC to the **semiconductor** substrate of said chip 5. Thereafter, they are integrally molded with resin, and the part of broken lines is **cut**, thereby fixing said chips 4 and 5 on the mounting parts 2 and 3 insulated from each other.

28/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014414344
WPI Acc No: 2002-235047/200229
Related WPI Acc No: 1999-312335; 1999-619070; 1999-619757; 2000-086254; 2001-089681; 2001-122024; 2002-225557; 2002-370324; 2003-844365
XRPX Acc No: N02-180379
Integrated circuit package e.g. DRAM **semiconductor** memory package, arranges interdigitated leads closely from edge-to-edge across front surface of integrated circuit **die**
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: BROOKS J M; SCHOENFELD A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6271582	B1	20010807	US 97827886	A	19970407	200229	B

Priority Applications (No Type Date): US 97827886 A 19970407
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6271582	B1		18	H01L-029/41	

Abstract (Basic): US 6271582 B1
Abstract (Basic):
NOVELTY - Lead-on-chip (LOC) **lead frame** (22) has **several** interdigitated **leads** (24). A portion of each lead extends closely across front surface of integrated circuit (IC) **die** (28) from one edge to opposite edge. A double-sided adhesive tape (30) secures the IC **die** to LOC **lead frame**.
USE - E.g. DRAM **semiconductor** memory package.
ADVANTAGE - By extending the leads from edge-to-edge across the front surface closely, a substantial front surface **area** is adhesively **attached** to the leads through the tape. Hence, the support of IC **die** is improved and the conduction of heat away from IC **die** through the LOC **lead frame** is also improved.
DESCRIPTION OF DRAWING(S) - The drawing shows the isometric **cut**-away view of IC **die** package having interdigitated LOC **lead frame**.
LOC **lead frame** (22)
interdigitated leads (24)
IC **die** (28)
adhesive tape (30)
pp; 18 DwgNo 2/10

28/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014358152
WPI Acc No: 2002-178853/200223
Related WPI Acc No: 1999-203963; 2000-557520; 2000-627920; 2002-054362; 2002-138236; 2002-163055; 2002-279757; 2002-291189; 2004-096661; 2004-096662; 2004-096663
XRAM Acc No: C02-055354
XRPX Acc No: N02-136008
Manufacture of plastic **lead frame** structure for

semiconductor devices, involves forming plastic **lead** **frame** structure from polymeric material, and coating frame structure with conductive material

Patent Assignee: JIANG T (JIAN-I); KING J L (KING-I); MICRON TECHNOLOGY INC (MICR-N)

Inventor: JIANG T; KING J L

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010051397	A1	20011213	US 97878935	A	19970619	200223 B
			US 98195765	A	19981118	
			US 2000639359	A	20000814	
			US 2001921535	A	20010803	
US 6544820	B2	20030408	US 97878935	A	19970619	200327
			US 98195765	A	19981118	
			US 2000639359	A	20000814	
			US 2001921535	A	20010803	

Priority Applications (No Type Date): US 97878935 A 19970619; US 98195765 A 19981118; US 2000639359 A 20000814; US 2001921535 A 20010803

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010051397	A1		9	H01L-021/44	Cont of application US 97878935
					Cont of application US 98195765
					Cont of application US 2000639359
					Cont of patent US 5879965
					Cont of patent US 6124151
					Cont of patent US 6294410
US 6544820	B2			H01L-021/44	Cont of application US 97878935
					Cont of application US 98195765
					Cont of application US 2000639359
					Cont of patent US 5879965
					Cont of patent US 6124151
					Cont of patent US 6294410

Abstract (Basic): US 20010051397 A1

Abstract (Basic):

NOVELTY - The method involves forming a plastic **lead** **frame** (10) structure from polymeric material, and coating the frame structure with a conductive material.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(i) manufacture of one or more portions of a **semiconductor** device. The method involves forming one or more conductive plastic **lead frame** having **several lead** fingers (12), by stamping and/or **etching** a conductive **lead frame**. A **semiconductor** device having several bond pads (14), is attached to a portion of one or more conductive plastic **lead frame**. One or more bond pads are connected to at least one lead finger. One or more portions of the **semiconductor** device and conductive plastic **lead frame**, are encapsulated; and

(ii) manufacture of circuit card. The method involves attaching one or more integrated circuit (IC) packages to a circuit card. One or more IC packages contain at least one conductive plastic **lead** **frame** formed by stamping and/or **etching**.

USE - The **lead frame** is used for packaging integrated circuits, and for manufacture of **semiconductor** devices and integrated circuits.

ADVANTAGE - Manufacturing cost of the plastic **lead** **frame** is reduced when compared with the manufacture of metal **lead frame**. Transparency, corrosion resistance and

oxidation resistance of the plastic or composite plastic **lead frame**, are enhanced. The **lead frame** maintains its characteristics necessary for use in commercial production of IC packages. The overall cost of IC chip packaging is reduced by using plastic **lead frames** coated with conductive layers. The use of transparent polymers and intrinsically conductive polymers facilitates ultraviolet (UV) or other light **source** cure of **die attach** materials. The methods used to produce such **lead frames** are simple and can be easily incorporated into existing high-speed production lines for manufacturing IC chips.

DESCRIPTION OF DRAWING(S) - The figure shows the perspective view of the **lead frame**.

Plastic **lead frame** (10)
Lead fingers (12)
Bond pads (14)
pp; 9 DwgNo 3/7

28/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008778948
WPI Acc No: 1991-282965/199139
XRPX Acc No: N91-216414
Resin seal type **semiconductor** device - supplies power by connecting pads to supply via bonding lead and is sealed by mould resin
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KOMENAKA K
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 447922	A	19910925	EP 91103751	A	19910312	199139	B
JP 3263334	A	19911122	JP 9062037	A	19900313	199202	
US 5089879	A	19920218	US 91667335	A	19910311	199210	
EP 447922	B1	19951115	EP 91103751	A	19910312	199550	
DE 69114554	E	19951221	DE 614554	A	19910312	199605	
			EP 91103751	A	19910312		

Priority Applications (No Type Date): JP 9062037 A 19900313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 447922	A				
	Designated States (Regional): DE FR GB				
EP 447922	B1	E	10	H01L-023/495	
	Designated States (Regional): DE FR GB				
DE 69114554	E			H01L-023/495	Based on patent EP 447922

Abstract (Basic): EP 447922 A

The **semiconductor** device, of the resin seal type known as DIP (Dual In-line Package), supplying electric signals or potential to several isolated pads comprises a **lead frame** (21) with **die** support (33) carrying **several leads** (43) arranged on the underside. A **semiconductor** chip (51) with pads (52) connected to the leads (43) by bonding wires (10) is **mounted** on the **die** support (33) and a wire lead (46) coupled to the power source crosses above the chip and supplies power to at least two of the pads.

The whole device is sealed by mould resin (11).

ADVANTAGE - Reduced noise. (5pp Dwg.No.1/11

Abstract (Equivalent): EP 447922 B

A resin-sealed **semiconductor** device comprising: a **lead frame** (21) having a chip support (33) on the central portion of the **lead frame** (21) and a plurality of leads (43) arranged around the periphery of the chip support (33), each lead having a bonding site at its inner end adjacent to said chip support; a **semiconductor** chip (51) mounted on the chip support (33) and having a plurality of contact pads (52) on its surface respective ones of said contact pads (52) being wire bonded to respective ones of said bonding sites of said leads (43); and moulded resin (11) sealing the **lead frame** (21), the **semiconductor** chip (51), and the wire lead (46), characterised in that a further lead portion (46) of said **lead frame** is connected to one of said leads (43) and extends above and across said surface of said **semiconductor** chip (51) to a bonding post (45) adjacent to said chip support, said bonding post (45) being connected by a wire bond to a further one of said contact pads (52) of said chip (51).

Dwg.1/11

Abstract (Equivalent): US 5089879 A

The resin seal type **semiconductor** device comprises a **lead frame** having a support and a number of leads, a **semiconductor** chip **mounted** on the **die** support and having a number of pads connected to the leads. Furthermore, the device has a wire lead arranged above the **semiconductor** chip.

For example, power source is supplied from the lead supplying power **source** to **one** of the pads receiving power source, by connecting the lead and the **one** pad. Furthermore, power **source** is supplied from the lead to another pad located far from the one pad by connecting the lead and the another pad through the wire lead.

USE - DIP (Dual In-Line Package). (8pp

32/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

04336602 INSPEC Abstract Number: B9303-0170J-033, C9303-5490-002
Title: High performance, high density packaging (CRAY supercomputer)
Author(s): Steitz, R.R.; Christie, D.M.
Author Affiliation: Cray Research, Inc., Chippewa Falls, WI, USA
Conference Title: IEPS. Proceedings of the Technical Conference. 1992 International Electronics Packaging Conference p.788-94
Publisher: Int. Electron. Packaging Soc, Wheaton, IL, USA
Publication Date: 1992 Country of Publication: USA 2 vol. 1185 pp.
Conference Date: 27-30 Sept. 1992 Conference Location: Austin, TX, USA
Language: English
Abstract: The CRAY Y-MP C90 supercomputer system uses a new packaging technology which combines conventional packaging concepts with **semiconductor** technology to create a leading edge IC/package/board attach system, which can employ AlN for maximum heat dissipation. The package design incorporates a hermetically sealed, leadless chip carrier that attaches to a printed circuit board by a tape automated bonding (TAB) **leadframe** . In order to allow for maximum heat dissipation, the integrated circuit (IC) is silver/glass **die attached** at 425 degrees C for 30+or-10 minutes. Maximum circuit density is achieved by using a glass sealed lid on top of the metal traces of the chip carrier. This glass sealing operation is carried out at 425 degrees C for 15+or-5 minutes. This packaging scheme allows the state-of-the-art chip carrier to be only 0.604+or-0.005 inches on each side yet still have 360 traces which are aluminum on the inside edge and gold on the outside edge. This allows for ease of aluminum wirebonding from the silicon integrated circuit bonding pads to the chip carrier aluminum metallization. It also allows a gold-to-gold TAB bond to be performed in order to connect the chip carrier to the circuit board. The inner aluminium metallization is on a 4 mil pitch, and the outer gold metallization is on a 5 mil pitch. With a uniquely designed **area** TAB **attached**, this package occupies only 1.21 square inches on the circuit board.
Subfile: B C

32/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016098453
WPI Acc No: 2004-256329/200424
Related WPI Acc No: 2001-079093; 2002-234981; 2002-237576; 2004-141205; 2004-224848
XRPX Acc No: N04-203753
Adhesive coated material attaching method for lead-over-chip **semiconductor** device, involves advancing **leadframe** to position one site to receive one decal, and indexing **leadframe** to place another site to receive another decal
Patent Assignee: CHAPMAN G M (CHAP-I)
Inventor: CHAPMAN G M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040033642	A1	20040219	US 97908291	A	19970807	200424 B
			US 2000484852	A	20000118	
			US 2003639124	A	20030811	

Priority Applications (No Type Date): US 97908291 A 19970807; US 2000484852 A 20000118; US 2003639124 A 20030811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040033642	A1		27	H01L-021/48	Cont of application US 97908291 Cont of application US 2000484852 Cont of patent US 6096165 Cont of patent US 6623592

Abstract (Basic): US 20040033642 A1
Abstract (Basic):

NOVELTY - The method involves operating **two sources** to supply **two** lengths (212,230) of adhesively coated tape to an application apparatus. The apparatus includes two **dies** for cutting the two decals from the two tape lengths. An indexing apparatus advances a lead-over-chip **leadframe** to position a site to receive one decal and indexes the **leadframe** to position another site to receive another decal from the application apparatus.

USE - Used for applying adhesively coated tape material segments to **lead frames** lead-over-chip type **semiconductor** device assemblies.

ADVANTAGE - The method applies tape to a **lead frame** without wasting tape and the **die** sites are indexed to separate locations for the application of each tape segment without having to apply in a single punch operation to the desired **die** site of the **lead frame**.

DESCRIPTION OF DRAWING(S) - The drawing shows an exploded view of an application mechanism.

Base (160)
Front cross unit (166)
Rear cross unit (168)
Opening (170)
Punch guide insert (176)
Tape lengths (212,230)
pp; 27 DwgNo 3/18

32/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016066997
WPI Acc No: 2004-224848/200421
Related WPI Acc No: 2001-079093; 2002-234981; 2002-237576; 2004-141205; 2004-256329
XRAM Acc No: C04-088811
XRPX Acc No: N04-177628

Coating material applying system for **semiconductor die mounting** site comprises sources for applying adhesively coated materials, indexing apparatus for moving the **leadframes**, and application apparatus for receiving the **leadframes**

Patent Assignee: CHAPMAN G M (CHAP-I)
Inventor: CHAPMAN G M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040026044	A1	20040212	US 97908291	A	19970807	200421 B
			US 99330794	A	19990614	
			US 2001875632	A	20010606	
			US 2003633926	A	20030804	

Priority Applications (No Type Date): US 97908291 A 19970807; US 99330794 A 19990614; US 2001875632 A 20010606; US 2003633926 A 20030804
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040026044 A1			28	B32B-031/00	Div ex application US 97908291 Cont of application US 99330794 Cont of application US 2001875632 Div ex patent US 6096165 Cont of patent US 6267167 Cont of patent US 6607019

Abstract (Basic): US 20040026044 A1
Abstract (Basic):

NOVELTY - A coating material applying system (104) comprises **first** and **second sources** (106) for applying adhesively coated materials, indexing apparatus for moving the **leadframes** relative to application apparatus (108) in a single **leadframe** (138), and application apparatus for receiving the **leadframes** in **leadframe**-by-**leadframe** sequence in a continuous manner.

DETAILED DESCRIPTION - A coating material applying system comprises **first** and **second sources** for applying adhesively coated materials, indexing apparatus, and application apparatus.

The **first source** for supplying a **first** length of adhesively coated material at first location of the first portion of the **semiconductor die mounting** site o the first **leadframe** in the continuous manner.

The **second source** for supplying a **second** length of adhesively coated material at a second location of the second portion of the **semiconductor die mounting** site of the second **leadframe** of the **leadframes** in a continuous manner.

The indexing apparatus includes an apparatus for moving the **leadframes** relative to the application apparatus in a single **leadframe** by single **leadframe** movement of the **leadframes** in continuous manner.

The application apparatus includes first cutting structure, second cutting structure, and operation apparatuses for moving the respective cutting **dies**. The first cutting structure receives the first cutting **die** that can be moved relative to the first cutting structure for receiving the first length of the adhesively coated material.

The second cutting structure receives the second cutting **die** that can be moved relative to the second cutting structure for receiving the second length of the adhesively coated material. The operation apparatuses move the cutting **dies** relative to the respective cutting structure for forming the respective increments and for urging the respective increments against the first or second location of the **semiconductor die mounting** site of the respective **leadframe**.

USE - For applying adhesively coated material to **semiconductor die mounting** site.

ADVANTAGE - The system allows the tape to be applied to a **leadframe** without washing tape and without having to apply the tape in single punch operation to the desired **die** site of the **leadframe**.

DESCRIPTION OF DRAWING(S) - The drawing shows a simplified depiction of the inventive system.

Coating material applying system (104)
Sources (106)

Application apparatus (108)
Drive rollers (122, 124)
Leadframe (138)
pp; 28 DwgNo 2/18

32/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015983355
WPI Acc No: 2004-141205/200414
Related WPI Acc No: 2001-079093; 2002-234981; 2002-237576; 2004-224848; 2004-256329
XRAM Acc No: C04-056238
XRPX Acc No: N04-112653
Attaching portions of adhesively coated material to sites on **leadframe** by supplying **leadframes** sequentially through application structure to apply two portions of adhesively coated material to two sites at two respective locations
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: CHAPMAN G M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6623592	B1	20030923	US 97908291	A	19970807	200414	B
			US 2000484852	A	20000118		

Priority Applications (No Type Date): US 97908291 A 19970807; US 2000484852 A 20000118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6623592	B1		26	B32B-031/00	Cont of application US 97908291 Cont of patent US 6096165

Abstract (Basic): US 6623592 B1
Abstract (Basic):
NOVELTY - Attaching portions of adhesively coated material to sites on a **leadframe** involves supplying several **leadframes** sequentially through an application structure (30) to apply a first portion of adhesively coated material to a first site at a first location and to apply a second portion of the adhesively coated material to a second site at a second location.
DETAILED DESCRIPTION - Attaching portions of adhesively coated material to sites on a **leadframe** (22-26) involves providing a source of an adhesively coated material (12, 16); providing a **leadframe** having a first site for attachment of a first portion of the adhesively coated material and a second site for attachment of a second portion of the adhesively coated material; providing an application apparatus having first and second applicators, where a displacement of the application apparatus operates to simultaneously displace the first applicator toward a first location and the second applicator toward a second location; providing an indexing apparatus for positioning the **leadframe** in a first condition such that the first site of the **leadframe** is situated at the first location, and for positioning the **leadframe** in a second condition such that the second site is situated at the second location; operating the indexing apparatus to displace the **leadframe** to the **first** condition; operating the **source** of the adhesively coated material to selectively supply the first applicator with the adhesively coated

material while withholding a supply of the adhesively coated material from the second applicator; displacing the application apparatus such that the first applicator is urged toward the first location to cause the first applicator to remove the first portion of the adhesively coated material from the source of adhesively coated material and apply the first portion to the first site while the second applicator is urged toward the second site without removing the second portion of the adhesively coated material from the **source** or applying the **second** portion of the second site; operating the indexing apparatus to displace the **leadframe** to the **second** condition; operating the **source** of the adhesively coated material to selectively supply the second applicator with adhesively coated material while withholding a supply of the adhesively coated material from the first applicator; displacing the application apparatus such that the second applicator is urged toward the second location to cause the second applicator to remove the second portion of the adhesively coated material from the **source** and apply the **second** portion to the second site while the first applicator is urged toward the first site without removing another portion of the adhesively coated material from the source or applying another portion to the first site.

USE - The method is used for attaching portions of adhesively coated material to several sites on at least two **leadframes**. It is particularly used for applying adhesively coated tape material segments, i.e. decals, to **leadframes** for **semiconductor** devices, particularly lead-over-chip type **semiconductor** device assemblies.

ADVANTAGE - The invention efficiently applies adhesive tape where desired on a **leadframe**, without wasting tape and without having to apply the tape in a single punch operation to the desired **die** site of the **leadframe**.

DESCRIPTION OF DRAWING(S) - The figure is a simplified depiction of the inventive system.

Source of an adhesively coated material (12, 16)

Leadframe (22-26)

Application structure (30)

Drive roller (46, 60)

pp; 26 DwgNo 1/18

32/3,AB/5 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015930957

WPI Acc No: 2004-088798/200409

XRAM Acc No: C04-036126

XRPX Acc No: N04-071088

Semiconductor device comprises **semiconductor** chip, base metal **lead frame**, copper wires, and resin molded member sealing the chip and a large portion of the **lead frame** and copper wires

Patent Assignee: TOSHIBA KK (TOKE); FUKATANI T (FUKA-I); MASUDA H (MASU-I); MOTONAMI K (MOTO-I)

Inventor: FUKATANI T; MASUDA H; MOTONAMI K

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030116837	A1	20030626	US 2002194296	A	20020715	200409	B
CN 1428853	A	20030709	CN 2002141229	A	20020628	200409	
JP 2003197827	A	20030711	JP 2001392695	A	20011225	200409	

Priority Applications (No Type Date): JP 2001392695 A 20011225
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030116837 A1 9 H01L-021/44
CN 1428853 A H01L-023/48
JP 2003197827 A 6 H01L-023/28

Abstract (Basic): US 20030116837 A1
Abstract (Basic):
NOVELTY - A **semiconductor** device has **semiconductor** chip; base metal **lead frame** with no residual of rust proof film; copper wires to directly connect electrodes on chip to inner ends of leads; and resin molded member to hermetically seal the chip, a large portion of the **lead frame**, and the copper wires.
DETAILED DESCRIPTION - A **semiconductor** device has **semiconductor** chip; base metal **lead frame** with no residual of rust proof film, including **die** pad **mounted** with the chip and leads disposed so that inner ends of the leads are positioned along periphery of **die** pad; copper wires to directly connect electrodes on chip to inner ends of leads; and resin molded member to hermetically seal the chip, a large portion of the **lead frame**, and the copper wires.
An INDEPENDENT CLAIM is also included for a method of manufacturing the **semiconductor** device comprising preparing the base metal **lead frame**; applying non-benzotriazole series rustproof agent on surface of **lead frame**; performing **die** -bonding for fixing the **semiconductor** chip of on the **die** pad in heated atmosphere by use of non-metal series paste; performing wire-bonding to connect the electrodes on the chip to the inner ends of the leads by use of copper wires; forming resin molded member by sealing the **lead frame** with resin; and forming leads protruding from the resin molded member.
USE - Used as **semiconductor** device.
ADVANTAGE - The invention reduces manufacturing costs in a way that it avoids the use of noble metals, and is capable of improving especially reliability of the resin molding with no harmful residue substance left in the process.
DESCRIPTION OF DRAWING(S) - The figure is a flow chart showing the process of the **semiconductor** manufacturing method.
pp; 9 DwgNo 2/6

32/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015861780
WPI Acc No: 2004-019610/200402
Related WPI Acc No: 2000-282405
XRAM Acc No: C04-006007
XRPX Acc No: N04-015023
Power **semiconductor** package includes bottom **leadframe**, second terminal, **semiconductor** power metal oxide **semiconductor** field effect transistor **die**, conductive plate, and beam portion coupled to the conductive plate
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: DELEON R; MUNOZ J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6396127	B1	20020528	US 98101810	P	19980925	200402 B
			US 2000476825	A	20000103	

Priority Applications (No Type Date): US 98101810 P 19980925; US 2000476825 A 20000103

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6396127	B1		14	H01L-023/50	Provisional application US 98101810

Abstract (Basic): US 6396127 B1

Abstract (Basic):

NOVELTY - A power **semiconductor** package includes:

(i) a bottom **leadframe** having a bottom plate and a first terminal;

(ii) a second terminal being co-planar with the first terminal;

(iii) a **semiconductor** power metal oxide **semiconductor** field effect transistor **die**;

(iv) a conductive plate coupled to and spanning a part of the first metallized region defining the source connection; and

(v) a beam portion that is coupled to the conductive plate to the second terminal

DETAILED DESCRIPTION - A power **semiconductor** package (110) includes:

(a) a bottom **leadframe** having a bottom plate (13) and a first terminal (12a) extending from the bottom plate;

(b) a second terminal (12b) being co-planar with the first terminal;

(c) a **semiconductor** power metal oxide **semiconductor** field effect transistor (MOSFET) **die** (16) having a bottom surface defining a drain connection and a surface on which a first metallized region (18) defining a **source** and a **second** metallized region defining a gate are disposed;

(d) a conductive plate coupled to and spanning a part of the first metallized region defining the source connection; and

(e) a beam portion (34) being sized and shaped to couple the conductive plate portion to the second terminal such that it is coupled to the source.

The bottom surface is coupled to the bottom plate of the **leadframe** such that first terminal is connected to the drain. The conductive plate includes a periphery and a chamfered edge at the periphery extending upward and away from the first metallized region. The peripheral edges define the periphery of the conductive plate. The beam portion extends from the peripheral edge of the metallized plate and is unitarily formed with the second terminal at a distal end. The chamfered edge is disposed at the peripheral edge from which the beam portion extends.

USE - Used as **semiconductor** package.

ADVANTAGE - The package provides a large contact area for coupling the terminal to the metallized region thus reducing resistance to current flow and reducing inductance, while providing improved performance at high frequency. The structure also provides a thermal path for heat to escape the **semiconductor die** through the strap member.

DESCRIPTION OF DRAWING(S) - The figure is a side view of the **semiconductor** package.

Terminal (12a)

Terminal (12b)

Bottom plate (13)

MOSFET **die** (16)

Metallized region (18)
Beam portion (34)
Curable conductive layer (46)
Semiconductor package (110)
pp; 14 DwgNo 3/15

32/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015789366
WPI Acc No: 2003-851569/200379
Related WPI Acc No: 2003-801182
XRAM Acc No: C03-239862
XRPX Acc No: N03-680068
Wireless bonded **semiconductor** device, e.g. insulating gate bipolar transistor, has **lead frame** with expanded mounting face at one end and connecting-pin, and **semiconductor** chip mounted on metal **lead frame**
Patent Assignee: CHINO EXCEL TECHNOLOGIES CORP (CHIN-N)
Inventor: CHIEN F; DUNG J; LI Y; TU K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030095393	A1	20030522	US 2002245333	A	20020918	200379	B

Priority Applications (No Type Date): TW 2001128580 A 20011119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030095393	A1		11	H01R-009/00	

Abstract (Basic): US 20030095393 A1
Abstract (Basic):

NOVELTY - A wireless bonded **semiconductor** device has **lead frame** with expanded mounting face at one end and a connecting-pin terminal leading out from it; and **semiconductor** chip mounted on the metal **lead frame** and contains a contact connected to the **lead frame** and a connecting-pin terminal leading out from its bottom face, and a contact and individual connecting-pin terminals leading out from its top face.

DETAILED DESCRIPTION - A wireless bonded **semiconductor** device (1) includes a **lead frame** (2) having an expanded mounting face (20) at one end and a connecting-pin terminal (21-23) leading out from it; and a **semiconductor** chip (3) mounted on the metal **lead frame** and contains a contact connected to the **lead frame** and a connecting-pin terminal leading out from its bottom face, and a contact and individual connecting-pin terminals leading out from its top face, such that no metal bonding wire exist between the surface contact and individual connecting-pin terminal, instead a matrix of the connecting-pin terminal with pre-determined extension length that folded and bonded onto the surface contact of the **semiconductor** is used.

An INDEPENDENT CLAIM is also included for packaging a wireless bonded **semiconductor** device by:

(i) rolling a conductive metal matrix to form a shape of **lead frame** which is provided with an expanded mounting face at one end and connecting-pin terminal at the other end;

(ii) rolling the shape of **lead frame** into a three-dimensional (3-D) frame to form a connecting-pin terminal and an expanded mounting face in different planes, and to form separate

individual connecting terminals in vertical arrangement with respect to the expanded mounting face;

(iii) attaching a **semiconductor** chip to the expanded mounting face so that a contact on the bottom face of the chip is connected to the **lead frame**;

(iv) passing the **semiconductor** device through a solder oven to dip solder balls onto the surface contacts of the **semiconductor** chip;

(v) folding and pressing the separate individual connecting-pin terminals toward the center; contacting the surface contacts of the chip and passing the **semiconductor** device through a bake oven for heating and pressurizing so that the solder balls are melted to form electrical connections and then insulating adhesive is sprayed onto the surface and supporting piece is **cut** off; and

(vi) packaging the **semiconductor** device with a ceramic or plastic molding material (5).

USE - Used as bonded **semiconductor** device, e.g. TO (sic) packaged metal-oxide -**semiconductor** power transistor, insulating gate bipolar transistor, bi-carriers junction transistor, power diode, or rectifier.

ADVANTAGE - The formation of metal soldering wire between the surface contact and individual connecting-pin terminals is omitted, while increasing the **attached area** and resulting in connecting-pin terminal with increased area so that the ON-resistance can be reduced, the ON-current can be increased, and heat can be further reduced, thus increasing the yield while reducing the cost.

DESCRIPTION OF DRAWING(S) - The figure is a schematic view of the wireless bonded **semiconductor** device.

Semiconductor device (1)
Lead frame (2)
Semiconductor chip (3)
Plastic molding material (5)
Mounting face (20)
Connecting-pin terminal (21-23)
pp; 11 DwgNo 1/2

32/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015738981
WPI Acc No: 2003-801182/200375
Related WPI Acc No: 2003-851569
XRAM Acc No: C03-221159
XRPX Acc No: N03-642024
Wireless bonded **semiconductor** device includes matrix of connecting-pin terminals with pre-determined extension length that directly folded and bonded into surface contact of **semiconductor** chip
Patent Assignee: CHINO-EXCEL TECHNOLOGY CORP (CHIN-N)
Inventor: DUNG J; JIAN F; LI Y; TU G; CHIEN F; TU K; TUNG C
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030094678	A1	20030522	US 2002298978	A	20021118	200375	B
TW 504816	A	20021001	TW 2001128579	A	20011119	200375	
TW 529145	A	20030421	TW 2001128580	A	20011119	200375	

Priority Applications (No Type Date): TW 2001128580 A 20011119; TW

2001128579 A 20011119

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030094678	A1		11	H01L-023/495	
TW 504816	A			H01L-023/28	
TW 529145	A			H01L-023/495	

Abstract (Basic): US 20030094678 A1

Abstract (Basic):

NOVELTY - A wireless bonded **semiconductor** device comprises a **lead frame**, and a **semiconductor** chip mounted on the **lead frame**. A matrix of connecting-pin terminals with pre-determined extension length that directly folded and bonded into the surface contact of the **semiconductor** chip is employed.

DETAILED DESCRIPTION - A wireless bonded **semiconductor** device (1) comprises a **lead frame** (2), and a **semiconductor** chip (3) mounted on the **lead frame**. The chip contains contact(s) electrically connected to the **lead frame** and a connecting-pin terminal (21) leading out from its bottom face and contact(s) and individual connecting-pin terminals (22, 23) leading out from its top face. A matrix of connecting-pin terminals with pre-determined extension length that directly folded and bonded into the surface contact of the **semiconductor** chip is employed.

An INDEPENDENT CLAIM is also included for a method of packaging a wireless bonded **semiconductor** device comprising:

(a) rolling the shape of **lead frame** into 3D **lead frame**;

(b) attaching a **semiconductor** chip to an expanded mounting face (20) of the **lead frame**;

(c) passing the **semiconductor** device through a solder oven so as to dip solder balls into the surface contacts of the chip;

(d) folding and pressing separate individual connecting-pin terminals toward the center; and

(e) contacting the surface contacts of the chip and passing the device through a bake oven for heating and pressuring so that the solder balls are melted to form electrical connections with individual connecting-pin terminals and then insulating adhesive is sprayed into the surface and the supporting piece is **cut** off, finally, packaging the **semiconductor** device with a ceramic or a plastic molding material.

USE - Used as wireless bonded **semiconductor** device of high current power transistors, e.g. MOSFET, insulating gate bipolar transistor, bi-carriers junction transistor, a power diode or rectifier.

ADVANTAGE - No metal bonding wire exist between the surface contact and individual connecting-pin terminals, while increasing **attached area** and resulting in a connecting-pin terminal with increased area so that ON-resistance can be reduced, ON-current can be increased, and heat can be further reduced. This simplifies manufacturing process and increases yield so as to further reduce cost.

DESCRIPTION OF DRAWING(S) - The figure is a schematic view showing a wireless bonded **semiconductor** device.

Semiconductor device (1)
Lead frame (2)
Semiconductor chip (3)
Expanded mounting face (20)
Connecting-pin terminal (21)
Connecting-pin terminals (22, 23)
pp; 11 DwgNo 1/2

32/3,AB/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015703693
WPI Acc No: 2003-765886/200372
XRAM Acc No: C03-210360
XRPX Acc No: N03-613441
Dual **die** bonder device for **semiconductor** device with two **semiconductor dies** has two **die**-bonding sections located in two respective halves of transfer rail to respectively **die**-bond the **dies** with liquid adhesive and insulating adhesive tape
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); AHN S C (AHNS-I); CHO K B (CHOK-I); HONG S B (HONG-I); KIM H S (KIMH-I)
Inventor: AHN S C; CHO G B; HONG S B; KIM H S; CHO K B
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030145939	A1	20030807	US 2002247316	A	20020920	200372	B
JP 2003243430	A	20030829	JP 200321860	A	20030130	200372	
KR 2003066983	A	20030814	KR 20026766	A	20020206	200382	

Priority Applications (No Type Date): KR 20026766 A 20020206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030145939	A1		8	B32B-031/00	
JP 2003243430	A		6	H01L-021/52	
KR 2003066983	A			H01L-023/48	

Abstract (Basic): US 20030145939 A1
Abstract (Basic):
NOVELTY - Dual **die** bonder device for a **semiconductor** device having two **semiconductor dies** comprises a transfer rail to transfer a substrate having **die**-bonding area(s), and two **die**-bonding sections respectively located in two halves of the transfer rail for respectively **die**-bonding the two **semiconductor dies** with a liquid adhesive and with an insulating adhesive tape.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of dual bonding two **semiconductor dies**, which comprises placing a first wafer (40) having first **semiconductor dies** (42) on a first wafer table (33) and a second wafer (60) having second **semiconductor dies** (62) on a second wafer table (55), placing a liquid adhesive on a **die** bonding area (14) of a substrate (12) located on a transfer rail (22) in a first bonding area by a liquid adhesive provider, transferring one of the first **dies** onto the liquid adhesive on the **die** bonding area by a **die** bonding tool, moving the substrate along the transfer rail to a second bonding **area**, **attaching** an insulating adhesive tape to the first **semiconductor die** or to the substrate by a tape attaching tool, and transferring one of the second **dies** onto the insulating adhesive tape by a second **die** bonding tool.
USE - The dual **die** bonder device is used for bonding two **semiconductor dies** to form a **semiconductor** device (claimed).
ADVANTAGE - The inventive dual **die** bonder device can perform in sequence two separate **die**-bonding processes using a liquid adhesive and an adhesive tape in a single apparatus, thus promoting

efficiency, improving productivity, and simplifying the manufacturing process. It requires less space and less time to perform the two separate adhesion processes. It reduces manufacturing costs by providing a device capable of adhering two **dies** with two different mediums.

DESCRIPTION OF DRAWING(S) - The figure is a perspective view showing the dual **die** bonder device.

Substrate (12)
Die bonding area (14)
Substrate magazine (21)
Transfer rail (22)
Liquid adhesive provider (31)
Liquid adhesive (32)
First wafer table (33)
First **die**-bonding tool (35)
First wafer (40)
First **semiconductor dies** (42)
Reel (52)
Tape-attaching tool (53)
Tape cutter (54)
Second wafer table (55)
Rollers (56)
Second **die**-bonding tool (57)
Tape holder (58)
Insulating adhesive tape (59)
Second wafer (60)
Second **semiconductor dies** (62)
pp; 8 DwgNo 3/3

32/3,AB/10 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014967934
WPI Acc No: 2003-028448/200302
XRAM Acc No: C03-006535
XRPX Acc No: N03-022315
Semiconductor package comprises **lead frame** and strap with its inner surface in electric contact with **semiconductor die** received in a nest of the **lead frame**
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: ANDERSON R; PAVIER M; SAMMON T
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020096749	A1	20020725	US 2001263137	P	20010122	200302	B
			US 200245809	A	20020111		
US 6717260	B2	20040406	US 2001263137	P	20010122	200425	
			US 200245809	A	20020111		

Priority Applications (No Type Date): US 2001263137 P 20010122; US 200245809 A 20020111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020096749	A1		6	H01L-023/495	Provisional application US 2001263137
US 6717260	B2			H01L-023/34	Provisional application US 2001263137

Abstract (Basic): US 20020096749 A1

Abstract (Basic):
NOVELTY - **Semiconductor** package comprises:
(1) **semiconductor die;**
(2) **lead frame** with strap cupped out of the frame plane to provide nest for a silicon **die;** and
(3) housing molded over and protecting the **lead frame** and silicon **die.**
The strap inner surface is in electric contact with one of the opposite surfaces of the **semiconductor die.** The other **die** surface is exposed for surface mounting connection with support surface.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for manufacturing the inventive **semiconductor** package.
USE - As a **semiconductor** package.
ADVANTAGE - The invention reduces the area or foot print of the **lead frame,** and reduces **lead frame** scrap. It has excellent thermal and electrical properties with reduced parasites, and can be made with inexpensive and reliable techniques. It can be easily bonded to support surfaces and is an ultra thin package.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a single **die mounted** in a chip.
Lead frame (30)
Strap (39)
Semiconductor die (44)
pp; 6 DwgNo 6/6

32/3,AB/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014212411
WPI Acc No: 2002-033108/200204
Related WPI Acc No: 1998-119394; 2004-068193
XRAM Acc No: C02-009145
XRPX Acc No: N02-025439
Fabrication of **semiconductor** components, e.g. ball grid array packages, involves cutting decals from ribbons of adhesive tape and **attaching semiconductor dies** to substrates using the decals
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: VANNORTWICK J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6281044	B1	20010828	US 95509048	A	19950731	200204 B
			US 9833497	A	19980302	
			US 99356267	A	19990716	

Priority Applications (No Type Date): US 99356267 A 19990716; US 95509048 A 19950731; US 9833497 A 19980302
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6281044	B1		17	H01L-021/58	Cont of application US 95509048
					CIP of application US 9833497
					CIP of patent US 6025212

Abstract (Basic): US 6281044 B1
Abstract (Basic):
NOVELTY - A **semiconductor** component is fabricated by cutting

decals from ribbons of adhesive tape, and then **attaching** a **semiconductor die** to a substrate using the decals.

DETAILED DESCRIPTION - Fabrication of a **semiconductor** component comprises:

(a) providing a **semiconductor die** (10);

(b) providing a substrate (14) comprising a polymer material;

(c) providing an adhesive tape of a predetermined width;

(d) providing a tape cutter apparatus for forming decals (52) with a first finished dimension equal to the width of the tape, and a second finished dimension equal to an indexed length of the tape;

(e) forming the decal using the tape cutter apparatus;

(f) attaching the decal to the substrate; and

(g) **attaching** the **die** to the substrate using the decals.

USE - For fabricating **semiconductor** components, e.g. ball grid array package or multi chip module (claimed).

ADVANTAGE - The invention makes decals without wasted tape, and with accurate alignment of the decal, the substrate, and the **die** to one another.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of a ball grid array package.

Semiconductor die (10)

Substrate (14)

Decals (52)

pp; 17 DwgNo 2c/8

32/3,AB/12 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014158093

WPI Acc No: 2001-642321/200174

XRPX Acc No: N01-480363

Paste dispenser for **die** bonding, comprises nozzle **connected** to pump which selectively discharges paste and cleaning liquid from corresponding containers

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001239196	A	20010904	JP 200053038	A	20000229	200174	B

Priority Applications (No Type Date): JP 200053038 A 20000229

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001239196	A		8	B05C-005/00	

Abstract (Basic): JP 2001239196 A

Abstract (Basic):

NOVELTY - A nozzle (18) is connected to a discharge pump (16A) which supplies paste (7) from the paste container (26A), to the chip **attachment area** of substrate (6). The paste flow path is then washed by the cleaning liquid supplied from a cleaning liquid container (26B), through discharge pump.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for paste coating method.

USE - For attaching **semiconductor** chip to substrate such as **lead frame**, in **die** bonding process.

ADVANTAGE - The washing operation is performed easily by supplying

cleaning liquid through discharge pump.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the paste dispenser. (Drawing includes non-English language text).

Substrate (6)
Paste (7)
Discharge pump (16A)
Nozzle (18)
Paste container (26A)
Cleaning liquid container (26B)
pp; 8 DwgNo 2/7

32/3,AB/13 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014056695
WPI Acc No: 2001-540908/200160
Related WPI Acc No: 2000-363552
XRAM Acc No: C01-161359
XRPX Acc No: N01-402015

Fabrication of **semiconductor** package involves using substrate having mask defining open **die attach area**

Patent Assignee: JIANG T (JIAN-I); SCHROCK E (SCHR-I)
Inventor: JIANG T; SCHROCK E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010013642	A1	20010816	US 98191215	A	19981112	200160	B
			US 99258961	A	19990301		

Priority Applications (No Type Date): US 98191215 A 19981112; US 99258961 A 19990301
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010013642	A1		13	H01L-023/495	Div ex application US 98191215 Div ex patent US 6048755

Abstract (Basic): US 20010013642 A1
Abstract (Basic):

NOVELTY - A **semiconductor** package is fabricated by providing a substrate having first surface (44) with **die attach area**, depositing photoimageable mask material on substrate (56), exposing and developing the mask material to form mask with an opening on the **die attach area**, placing a **semiconductor die** in the opening, and bonding the **die attach area**.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) a **semiconductor lead frame** comprising a substrate having surfaces, conductors formed on a first surface, a first mask formed on the first surface having via openings to the conductors, and a second mask formed on second surface comprising opening defining a **die attach area** on the substrate; and

(B) a substrate for fabricating a **semiconductor** package.

USE - The method is used for fabricating **semiconductor** package.

ADVANTAGE - The open **die attach area** permits the **die** to bonded directly to the substrate than to the solder mask.

This improves adhesion of the **die** to the substrate, reduces trapped moisture, and prevents delamination of the solder mask in the **die attach area.**

DESCRIPTION OF DRAWING(S) - The figure is a plan view of a panel containing substrate.

First surface (44)

Substrate (56)

pp; 13 DwgNo 2A/7

32/3,AB/14 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013595131

WPI Acc No: 2001-079338/200109

Related WPI Acc No: 2000-052202; 2001-190989; 2001-233982; 2001-353203; 2001-496225; 2002-224066; 2003-811053

XRAM Acc No: C01-022655

XRPX Acc No: N01-060368

Semiconductor device packaging process, for e.g. three dimension lead package, involves configuring outer leads to desired shape after removing molded polymeric package from mold assembly

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: TANDY P W

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6146919	A	20001114	US 97890414	A	19970709	200109 B
			US 99336919	A	19990621	

Priority Applications (No Type Date): US 97890414 A 19970709; US 99336919 A 19990621

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6146919	A		60	H01L-021/44	Div ex application US 97890414
					Div ex patent US 5986209

Abstract (Basic): US 6146919 A

Abstract (Basic):

NOVELTY - The **semiconductor die lead frame** assembly is aligned in a cavity of a mold assembly such that at least one of leads that are electrically **connected** to **semiconductor die** is adjacent to bottom plate (116) of mold assembly. The mold assembly is closed by injecting fluid polymeric encapsulant in the cavity of mold assembly. The molded polymeric package (120) is removed from mold assembly after curing encapsulant and outer leads (118) of package are configured to desired shape.

DETAILED DESCRIPTION - The **semiconductor die lead frame** assembly having electrical **connection** between **semiconductor die** and leads of **lead frame** is aligned in a cavity of mold assembly such that at least one lead is adjacent to bottom plate of mold assembly. The mold assembly is closed by injecting fluid polymeric encapsulant. The encapsulant is cured and a molded polymeric package (120) is removed from the mold assembly. Flash residue are removed from the **attachment area** of outer leads (118) by de-flashing bottom of the molded polymeric package and portions of outer leads. The outer leads are separated by lancing the **semiconductor die leadframe**. The **attachment area** of outer leads is plated with tin. The portions of molded

polymeric package that are adjacent and parallel to intermediate portion (112) of lead, are excised after which outer leads are configured to desired configuration.

USE - Used for packaging **semiconductor** device of chip-over-leads (COL) and leads-over-chip (LOC) configuration, and for manufacture of three dimensional lead (TDL) package.

ADVANTAGE - By suitably configuring the outer leads to desired shape after excising the portion of polymeric molded material corresponding to intermediate portion of lead, package size is reduced and bonding of device to external apparatus is improved.

DESCRIPTION OF DRAWING(S) - The figure shows cross-section of two bottom leaded packaged **semiconductor** device.

Bottom plate (116)
Outer leads (118)
Molded polymeric package (120)
pp; 60 DwgNo 5/18

32/3,AB/15 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013594886
WPI Acc No: 2001-079093/200109
Related WPI Acc No: 2002-234981; 2002-237576; 2004-141205; 2004-224848; 2004-256329
XRPX Acc No: N01-060137

Adhesive tape attachment method for **semiconductor** device involves cutting portions of adhesive tape by application structure for application to predetermined **die** locations of LOC **lead frame**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: CHAPMAN G M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6096165	A	20000801	US 97908291	A	19970807	200109	B

Priority Applications (No Type Date): US 97908291 A 19970807
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6096165	A		25	B32B-031/00	

Abstract (Basic): US 6096165 A

Abstract (Basic):

NOVELTY - LOC **lead frames** (22-26) are sequentially supplied to an application structure (20) that provides an adhesive tape to the predetermined locations of each **lead frame**. The application structure has a cutting **die** for cutting predetermined portions from the corresponding lengths (14,18) of the adhesive tape to be applied to the corresponding locations of the **semiconductor die** site of each LOC **lead frame**.

DETAILED DESCRIPTION - The method involves providing number of LOC **lead frames** in a **lead frame**-by-**lead frame** sequence, such that each **lead frame** has attachment site of a **semiconductor die**. An indexing structure (20) supplies the LOC **lead frames** in a **lead frame**-by-**lead frame** sequence to the direction of the application structure. **Two** adhesive tape **sources** (12,16) are operated to supply the predetermined lengths of the adhesive tape to the application structure.

USE - Applicable for attachment of portion of adhesive tape to lead over chip (LOC) of **semiconductor** device.

ADVANTAGE - Enables application of adhesive tape to desired **semiconductor die** location of **lead frame** without wasting tape and without enabling adhesive tape application in a single punch operation.

DESCRIPTION OF DRAWING(S) - The figure shows the system diagram for adhesive tape attachment.

Adhesive tape sources (12,16)
Adhesive tape lengths (14,18)
Application structure (20)
Indexing structure (20)
LOC **lead frames** (22-26)
pp; 25 DwgNo 1/18

32/3,AB/16 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013074748
WPI Acc No: 2000-246620/200021
Related WPI Acc No: 2000-246607
XRAM Acc No: C00-074666
XRPX Acc No: N00-184442

Wiring substrate for accepting an integrated circuit, comprises an outer layer with inner and outer surfaces, and a conductive layer with a second region having a coefficient of thermal expansion lesser than the first region

Patent Assignee: KULICKE & SOFFA HOLDINGS INC (KULI-N)
Inventor: BEILIN S I; CHAZAN D; KAMATH S
Number of Countries: 088 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200011919	A1	20000302	WO 99US18926	A	19990817	200021	B
AU 9960198	A	20000314	AU 9960198	A	19990817	200031	
US 6317331	B1	20011113	US 9897066	A	19980819	200173	
			US 99375175	A	19990816		

Priority Applications (No Type Date): US 99375175 A 19990816; US 9897066 P 19980819
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200011919	A1	E	21	H05K-001/02	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9960198	A	H05K-001/02	Based on patent WO 200011919	
US 6317331	B1	H05K-001/18	Provisional application US 9897066	

Abstract (Basic): WO 200011919 A1
Abstract (Basic):

NOVELTY - Multilayer wiring substrate comprises an outer layer (86) with an inner surface and an outer surface, with the outer surface having an attachment for mounting an integrated circuit; and a conductive layer laminated to the inner surface of the outer layer and which has two regions, with the coefficient of thermal expansion (CTE)

of the second region less than the first region.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for: an electronic assembly comprising:

(i) a printed wiring substrate (80) having a surface with a chip **attachment area**, a dielectric layer (84) having a first CTE, and a first thermal expansion reduction insert (82) opposite the chip **attachment area**, with the first thermal expansion reduction insert having a second CTE that is less than that first CTE;

(ii) a first integrated circuit (IC)(44) being mounted (preferably with a ball array) on the surface of the printed wiring substrate in the chip **attachment area**, with the first IC including a **semiconductor** chip having a third CTE and a second thermal expansion reduction insert having a fourth CTE; and

(iii) a second IC mounted (preferably with a ball array) on the second chip **attachment area** of the first IC.

USE - The wiring substrate, e.g. laminated printed circuit board, thin film circuit, **lead frame** or chip carriers is used to accept an integrated circuit, e.g. a **die**, a flip chip, or a ball-grid arrays (BGA) package.

ADVANTAGE - The invention provides wiring substrate with reduced thermal expansion.

DESCRIPTION OF DRAWING(S) - The figure shows a multilayer printed circuit board with a low CTE beneath an IC mounted on the PWB.

integrated circuit (44)
printed circuit board (80)
thermal expansion reduction insert (82)
dielectric layer (84)
outer layer (86)
pp; 21 DwgNo 3/5

32/3,AB/17 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012925761
WPI Acc No: 2000-097597/200008
XRAM Acc No: C00-028351
XRPX Acc No: N00-075420
Package for **semiconductor** devices e.g. power metal oxide **semiconductor** field-effect transistors
Patent Assignee: FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: BAJE G S; BENCUYA I; ESTACIO M C B; MALIGRO R D; SNAPP S P; TANGPUZ C N; SAPP S P
Number of Countries: 023 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9965077	A1	19991216	WO 99US12411	A	19990603	200008	B
TW 423136	A	20010221	TW 99109550	A	20000103	200138	
JP 2002518830	W	20020625	WO 99US12411	A	19990603	200243	
			JP 2000553996	A	19990603		
US 6423623	B1	20020723	US 9888651	A	19980609	200254	
			US 98141184	A	19980827		

Priority Applications (No Type Date): US 98141184 A 19980827; US 9888651 P 19980609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9965077	A1	E	15	H01L-023/48	

Designated States (National): CN JP KR

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

TW 423136	A		H01L-023/495	
JP 2002518830	W	13	H01L-023/48	Based on patent WO 9965077
US 6423623	B1		H01L-021/44	Provisional application US 9888651

Abstract (Basic): WO 9965077 A1

Abstract (Basic):

NOVELTY - A package comprises a silicon **die** (202) encapsulated by a protective molding, solder balls (204) in contact with a conductive layer on a top surface of the **die** and a first metal **lead frame** (206) extending outside the protective molding.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a packaging method for a silicon **die** (202) comprising disposing the solder balls (204) on the top surface of the **die**, bringing the first **lead frame** (206) in direct contact with the balls, directly attaching the substrate side of the **die** to the second **lead frame** (200) using a **die attach** process and encapsulating the **die** with a protective mold such that the first and second **lead frames** extend outside the mold.

USE - The package is for **semiconductor** devices e.g. power MOSFETs.

ADVANTAGE - Allows the size and shape of the **lead frame** to be tailored to fit the device and to minimize its electrical and thermal resistance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the wireless package.

drain **lead frame** (200)
silicon **die** (202)
solder balls (204)
source top **lead frame** (206)
gate top **lead frame** (208)
pp; 15 DwgNo 2/4

32/3,AB/18 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012733649
WPI Acc No: 1999-539766/199945
Related WPI Acc No: 1998-216516; 1999-166777; 2000-104893; 2001-353150; 2001-482562; 2003-029035
XRAM Acc No: C99-157668
XRPX Acc No: N99-399962
Laser wire bonding of wire embedded dielectrics to integrated circuit
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: EVERS S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5956607	A	19990921	US 96654192	A	19960528	199945	B
			US 97911389	A	19970814		

Priority Applications (No Type Date): US 96654192 A 19960528; US 97911389 A 19970814
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5956607	A		12	H01L-021/44	Div ex application US 96654192

Div ex patent US 5731244

Abstract (Basic): US 5956607 A
Abstract (Basic):
NOVELTY - The apparatus includes lasers with an optical arrangement which allows for each bond pad to be heated individually and simultaneously by a laser beam without having to move or scan the lasers.
DETAILED DESCRIPTION - **Semiconductor** device bonding apparatus comprises
(a) chip support defining a bonding location,
(b) at least **one** energy **source** mounted proximate the chip support,
(c) at least **one** energy **source** providing a number of energy beams,
(d) optical structure for directing the energy beams toward a number of bonding sites,
(e) chip component associated with the chip support.
USE - Wire bonding of **lead frames** to **semiconductor dice.**
ADVANTAGE - The use of laser heating reduces the mechanical limitations of the bonding process and the apparatus removes the need for moving the laser from bond to bond, and reduces bonding time.
DESCRIPTION OF DRAWING(S) - The drawing shows a boding apparatus.
lasers (12, 14, 16, 18)
laser beams (20, 22, 24, 26)
lenses (28, 30, 32, 34)
prisms (36, 38, 40, 42)
bonding sites (44, 46, 48, 50)
semiconductor chip (52)
lead finger (54)
optical flat (56)
chip support (58)
lead finger (68)
retaining members (72, 74)
resilient pad (76)
pp; 12 DwgNo 1/7

32/3,AB/19 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012612268
WPI Acc No: 1999-418372/199935
XRPX Acc No: N99-312301
Leadframe for integrated circuit (IC) package
Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: CHU C S; SPALDING P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5926695	A	19990720	US 97872658	A	19970610	199935	B

Priority Applications (No Type Date): US 97872658 A 19970610
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5926695	A		18	H01L-021/44	

Abstract (Basic): US 5926695 A

Abstract (Basic):
NOVELTY - The **leadframe** has a flow diverter for bifurcating the flow of encapsulant material during the molding of a **semiconductor** device package (300). The diverter is integrally formed with a **semiconductor die** support pad which is offset relative to the leads of the **leadframe**. The diverter is positioned adjacent a flow hole in the support pad and is angled upwardly relative to the support pad.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for:
(1) a packaged **semiconductor**,
(2) a method of manufacturing a **leadframe**, and
(3) a method of packaging a **semiconductor** device.
USE - For supporting a **die** and for providing conductive paths between the **die** and external circuitry in an IC package.
ADVANTAGE - Controls the amount of encapsulant material which is directed both above and below an **attached die** during the encapsulation process. Reduces or eliminates a pressure gradient between the upper and lower surfaces of the **die attach area** and reduces or eliminates problems associated with such a pressure gradient such as entrapped gas bubbles, **die attach area** misalignment, mechanical stress, poor heat transfer characteristics and reduced long term package reliability.
DESCRIPTION OF DRAWING(S) - The drawing shows a diagrammatic cross-sectional view of the encapsulated **semiconductor** device package.
package (300)
pp; 18 DwgNo 4G/5

32/3,AB/20 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012557110
WPI Acc No: 1999-363216/199931
XRPX Acc No: N99-271224
Semiconductor pellet positioning method on **lead frame** for **semiconductor** device manufacture - involves **etching** center section of electrically insulated portion for positioning and attaching pellet to **lead frame**
Patent Assignee: NEC KYUSHU LTD (KYUN)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11135524	A	19990521	JP 97296943	A	19971029	199931	B
JP 3037234	B2	20000424	JP 97296943	A	19971029	200025	

Priority Applications (No Type Date): JP 97296943 A 19971029
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11135524	A		5	H01L-021/52	
JP 3037234	B2		5	H01L-021/52	Previous Publ. patent JP 11135524

Abstract (Basic): JP 11135524 A
NOVELTY - Corresponding to the shape of **semiconductor** pellet (6), the center section of electrically insulated portion (2') joined with **lead frame** (1) is **etched. Semiconductor** pellet is then positioned in the **etched area** and **attached** to the **lead frame** using electroconductive glue (5).

USE - For attaching pellet on **lead frame** during **semiconductor** device manufacture.

ADVANTAGE - Reduces generation of inferior quality **semiconductor** device as contact of adjustment wire is limited.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram explaining the positioning process of pellet on **lead frame**.

(1) **Lead frame**; (2') Electrically insulated portion; (5) Electroconductive glue; (6) **Semiconductor** pellet.

Dwg.1/4

32/3,AB/21 (Item 20 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012513102

WPI Acc No: 1999-319208/199927

XRAM Acc No: C99-094218

XRPX Acc No: N99-239424

Moulding method of **semiconductor** device - involves removal of a gate remainder along a crack produced by pressing with a punch provided in the mould

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI DENKI ENG KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI ELECTRIC ENG CO LTD (MITQ)

Inventor: AOKI H; KATOU K; NISHITANI H; SEKIYA H

Number of Countries: 004 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11111745	A	19990423	JP 97270887	A	19971003	199927	B
CN 1213850	A	19990414	CN 98109714	A	19980605	199933	
KR 99036518	A	19990525	KR 9820615	A	19980603	200032	
US 6242287	B1	20010605	US 9844928	A	19980320	200133	
KR 323189	B	20020622	KR 9820615	A	19980603	200281	

Priority Applications (No Type Date): JP 97270887 A 19971003

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11111745	A		18	H01L-021/56	
CN 1213850	A			H01L-021/56	
KR 99036518	A			H01L-021/56	
US 6242287	B1			H01L-021/44	
KR 323189	B			H01L-021/56	Previous Publ. patent KR 99036518

Abstract (Basic): JP 11111745 A

NOVELTY - A crack is formed on a gate remainder (3b) which is extending from a sealing resin. The cracked gate remainder is removed along the crack by punching (11a).

DETAILED DESCRIPTION - The crack is made in the vertical direction. The **lead frame** and the gate punch are **mounted** on a frame **die** which is provided with a gate remainder accommodation portion. The gate punch touches the wall surface of the gate remainder accommodation portion. The gate punch is divided into top and bottom punch respectively. The **die** main surface is actuated by an elastic **attachment** provided. The **gate** remainder accommodation portion has a suction hole connected with a dust collector for collecting the resin pieces generated during punching.

INDEPENDENT CLAIMS are also included for (i) metallic mold for **semiconductor** molding. (ii) guide rail that conveys the **semiconductor** device to be sealed into the **lead frame**

. A gate relief groove is arranged along the longitudinal direction corresponding to the air vent of the metallic mold.

USE - For **semiconductor** molding.

ADVANTAGE - Since the gate remainder is removed along the crack the stress development near the base of the gate remainder is prevented. Scattering of the resin piece during gate crack is prevented by suction.

DESCRIPTION OF DRAWING - The figure explains the pinch **cut** process after a crack formation. (3b) Gate remainder; (11a) Bottom punch.

Dwg.10/38

32/3,AB/22 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012217515
WPI Acc No: 1999-023621/199902
XRPX Acc No: N99-018120
Integrated circuit with power distribution method - includes wires connecting power supply node to intermediate node and connecting intermediate node to another intermediate node
Patent Assignee: MOSEL VITELIC INC (MOSE-N); MOSEL VITELIC CORP (MOSE-N)
Inventor: LI L; LIU L C; MURRAY M A
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5838072	A	19981117	US 97805391	A	19970224	199902	B
TW 369700	A	19990911	TW 98102634	A	19980224	200035	

Priority Applications (No Type Date): US 97805391 A 19970224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5838072	A		6	H01L-023/28	
TW 369700	A			H01L-021/768	

Abstract (Basic): US 5838072 A

The integrated circuit (50) includes a supply node (53), comprising a bond pad, electrically connected to a power **source. Two** conductive wires (55a) lie external to and within the borders of a **semiconductor die.**

The wires each have one end connected to the supply node and the other end connected to a corresponding one of two intermediate nodes (54a) so that power from the power source is available at the intermediate nodes. A third wire (55b) connects one of the intermediate nodes to a third intermediate node (54b) so that power is available at the third node through the second.

ADVANTAGE - Allows power to be distributed without sacrificing valuable chip space and without requiring a special **lead frame.**

Dwg.5/5

32/3,AB/23 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011960997
WPI Acc No: 1998-377907/199832

XRPX Acc No: N98-295428

Attaching semiconductor die to transistor package - using temperature independent direct contact **die attach**, with resilient clamps used to **attach die** to **die attach area** of package

Patent Assignee: ERICSSON INC (TELF)

Inventor: LEIGHTON L C; MOLLER T W

Number of Countries: 081 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9828794	A1	19980702	WO 97US23098	A	19971212	199832	B
AU 9857024	A	19980717	AU 9857024	A	19971212	199848	
US 5877555	A	19990302	US 96771402	A	19961220	199916	
EP 953209	A1	19991103	EP 97953229	A	19971212	199951	
			WO 97US23098	A	19971212		
CN 1247636	A	20000315	CN 97181892	A	19971212	200031	
TW 412818	A	20001121	TW 97119321	A	19971219	200121	
KR 2000069623	A	20001125	WO 97US23098	A	19971212	200130	
			KR 99705625	A	19990619		
JP 2001507170	W	20010529	WO 97US23098	A	19971212	200136	
			JP 98528888	A	19971212		
KR 386787	B	20030609	WO 97US23098	A	19971212	200367	
			KR 99705625	A	19990619		

Priority Applications (No Type Date): US 96771402 A 19961220

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9828794	A1	E	24	H01L-023/66	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW				
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9857024	A			H01L-023/66	Based on patent WO 9828794
US 5877555	A			H01L-023/12	
EP 953209	A1	E		H01L-023/66	Based on patent WO 9828794
Designated States (Regional): DE ES FI FR GB IT NL SE					
CN 1247636	A			H01L-023/66	
TW 412818	A			H01L-021/60	
KR 2000069623	A			H01L-023/66	Based on patent WO 9828794
JP 2001507170	W		25	H01L-021/52	Based on patent WO 9828794
KR 386787	B			H01L-023/66	Previous Publ. patent KR 2000069623 Based on patent WO 9828794

Abstract (Basic): WO 9828794 A

A **semiconductor die**(22) is **attached** to a transistor package(20) by elastic clamps(26a-d), bonded between the top of the **die** the emitter, collector, or base **lead frame** (32,34) of the package.

The clamps provide a resilient force which causes the base of the **die** to make and maintain uniform contact with the **die attach area** of the package e.g. a mounting flange or non-conductive surface(30). The clamps are conductive and can conduct current from respective transistor cell locations on the **die** to the respective **lead frames** to which the clamps are bonded.

ADVANTAGE - **Attaches die** to substrate at relatively low temperature.

Dwg.3/5

32/3,AB/24 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011959910
WPI Acc No: 1998-376820/199832
Related WPI Acc No: 1997-511959; 1999-263224; 2001-564088
XRAM Acc No: C98-114280
XRPX Acc No: N98-294703
Non customised **die** assembly - involves assembling **dies** in a face-to-face configuration on a **lead-frame** with lead fingers of a variety of lengths, orientations and configurations
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: BRUCE J D; HABERSETZER D L; MA M K F; MILLER J E; ROBERTS G D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5770480	A	19980623	US 96664409	A	19960617	199832 B
			US 97833863	A	19970410	

Priority Applications (No Type Date): US 96664409 A 19960617; US 97833863 A 19970410
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5770480	A		13	H01L-021/44	Div ex application US 96664409 Div ex patent US 5677567

Abstract (Basic): US 5770480 A
A multi-**die** **semiconductor** assembly is formed by superimposing a pair of **dies** (502, 504) with different bond pad arrangements. A **leadframe** is provided with lead fingers (404) of different length, orientation and configuration and having a **die** paddle (402). Bond pads (516, 506) **area attached** on the first **die** to lead fingers on the first side, and on the second **die** to lead fingers on the second side. A passivation layer (514) may be included between the **dies**.
ADVANTAGE - **Dies** with different bond pad arrangements can be used in superimposed configuration to increase circuit density without the need for wire bonding.
Dwg.5/9

32/3,AB/25 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011908097
WPI Acc No: 1998-325007/199829
XRPX Acc No: N98-254232
Die attach material curing system for **attachment** of **semiconductor die** to **lead frame** - uses heat source for radiating thermal energy to carriers formed from highly thermal conductive material, similar to **lead frame** material, to attain desired temperature
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: AMADOR G; BUENDIA J S; HEINEN K G; STARK L E
Number of Countries: 028 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

EP 849773	A1	19980624	EP 97122428	A	19971218	199829	B
JP 10199904	A	19980731	JP 97349713	A	19971218	199841	
KR 98064248	A	19981007	KR 9769925	A	19971217	199949	
US 5993591	A	19991130	US 9632495	A	19961218	200003	
			US 97991128	A	19971216		
TW 370696	A	19990921	TW 97119140	A	19980303	200036	

Priority Applications (No Type Date): US 9632495 P 19961218; US 97991128 A 19971216

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 849773	A1	E	7	H01L-021/00	
Designated States (Regional): AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 10199904	A		6	H01L-021/52	
KR 98064248	A			H01L-021/48	
US 5993591	A			B32B-031/26	Provisional application US 9632495
TW 370696	A			H01L-021/60	

Abstract (Basic): EP 849773 A

The system includes a carrier receiving location for receiving at least one carrier (1) which contains at least one **leadframe** strip (3), a **die attach** material (15) on the **leadframe** strip and a **semiconductor die** (13) on the **die attach** material. A heat **source** (5) is provided for radiating thermal energy to the carrier receiving location, and a reflector (9) is disposed around the heat source and the carrier receiving location for reflecting thermal energy from the heat source to the carrier receiving location. The heat source may be a tungsten halogen lamp, providing radiation of energy in the range of from about 0.5 mW to about 2.0 mW. The system further comprises device responsive to a function of instantaneous temperature of the **die attach** material and the **leadframe** strip to control the intensity and profile of the heat source.

A source of flowing cool gas (11) is provided in heat exchange relationship with the reflector for cooling the reflector while heating the gas. The heated gas is passed through the carrier receiving location to provide a source of heat by convection at the carrier receiving location and purge the carrier receiving location of volatiles. The system further has at least one carrier at the carrier receiving location, containing at least one **leadframe** strip in it, a **die attach** material formed on the **leadframe** strip and a **semiconductor die** disposed on the **die attach** material. A second cool air inlet injects cooling air into the system upon completion of curing.

ADVANTAGE - Exhibits larger throughput than is available in prior art, quick response time of energy source, process is more flexible in terms of accommodating in-line processes, and allows modular assembly with minimum footprint. System is closed loop system, therefore provides temperature control. Continuous air flow provides relatively cleaner cure.

Dwg.1/2

32/3,AB/26 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011879296
WPI Acc No: 1998-296206/199826

XRPX Acc No: N98-231714
Lead frame for unitary construction **semiconductor** **die** packaging to reduce chip stress and deformation - has expansion **joint** for **connecting die** pad sections formed integrally with them
Patent Assignee: INST MICROELECTRONICS (MICR-N); UNIV SINGAPORE NAT (UYSI-N)
Inventor: BENG L T; BHANDARKAR S M; LIM T B
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SG 46955	A1	19980320	SG 951670	A	19951028	199826	B
US 5773878	A	19980630	US 96582643	A	19960104	199833	

Priority Applications (No Type Date): SG 951670 A 19951028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SG 46955	A1			H01L-023/495	
US 5773878	A			H01L-023/495	

Abstract (Basic): SG 46955 A
The **lead frame** comprises a **die** pad, a frame surrounding the **die** pad and **connected** to the **die** pad by **die** pad suspension straps, and a number of leads capable of being **connected** to a **semiconductor die**. The leads are formed integrally with the frame, and the **die** pad is divided into a number of sections, with adjacent sections connected by at least one expansion joint.
The **die** pad has a square shape which is divided into a number of sections, adjacent ones of which are connected by an expansion **joint**. The **die** pad may also be divided into two L-shaped sections connected by at least one expansion joint. The expansion joint comprises strip sections each **connected** to corresponding **die** pad section, respectively. The first and second strip sections are parallel, and the third strip section orthogonal to the first two strip sections, and connects them.
ADVANTAGE - Sectioned **die** pad allows relative motion between pad and chip during **die attach** cure, and breaks down total **die** pad **area** that is rigidly **attached** to chip into small sections, which reduce coefficient of thermal expansion mismatch, and out of plane deformation of assembly. Improves package mouldability and reduction in chip stress and deformation.

32/3,AB/27 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009864553
WPI Acc No: 1994-144413/199417
XRPX Acc No: N94-113733
Low inductance **lead frame** for **semiconductor** package - has **die attach area**, several intermediate connection bars positioned to be parallel to sides of **attach area**, and to be in plane displaced perpendicularly from **attach area**, and supports extend from **die** area
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: MOLINE D D; WEIR B E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5309019	A	19940503	US 9323407	A	19930226	199417	B

Priority Applications (No Type Date): US 9323407 A 19930226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5309019	A		5	H01L-023/48	

Abstract (Basic): US 5309019 A

The low inductance **lead frame** (10) is formed to have a **die attach area** (11). A number of intermediate connection bars (12,13,14,15) are positioned to be parallel to sides of the **die attach area** (11), and to be in a plane that is displaced perpendicularly from the **die attach area** (11). Each end of each intermediate connection bar is separated from an end of each other intermediate connection bar.

Supports (17) extend from the **die attach area** (11) to the intermediate connection bars to provide support for the intermediate connection bars. A number of leads (19,33,34) are positional in a plane and have a proximal end near the intermediate connection bars.

Dwg.1/2

32/3,AB/28 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009809123
WPI Acc No: 1994-088978/199411
XRAM Acc No: C94-040744
XRPX Acc No: N94-069826
Sealing **semiconductor** chip with resin - in which pouring stress of resin is charged according to change of viscosity of resin
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6039870	A	19940215	JP 92198555	A	19920724	199411	B

Priority Applications (No Type Date): JP 92198555 A 19920724
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6039870	A		4	B29C-045/02	

Abstract (Basic): JP 6039870 A

A sealing resin is poured into a seal gap until filled. During pouring of the resin, the pouring stress of the resin is changed according to the change of the viscosity of the resin. A sealing **die** is also claimed which has a sealing space and resin pouring stress adjuster.

A resin pouring stress adjusting plunger is **attached** to a **gate** connected to a runner connected to a pot of a lower **die**.

USE/ADVANTAGE - For sealing **semiconductor** chips mounted on **lead frames** set in **dies**, without causing voids or moving a bonding wire.

Dwg.1/3

32/3,AB/29 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009116456
WPI Acc No: 1992-243893/199230
XRPX Acc No: N92-186111
Semiconductor chip position detector - has film table supporting film through which **semiconductor** chips are illuminated from below, to highlight their positions for position detector or camera above table
Patent Assignee: SHARP KK (SHAF)
Inventor: NAEMURA J; OKANISHI M; YAMAZAKI M
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2251937	A	19920722	GB 9127441	A	19911227	199230	B
JP 4225537	A	19920814	JP 90408063	A	19901227	199239	
US 5307154	A	19940426	US 91812023	A	19911223	199416	
GB 2251937	B	19940803	GB 9127441	A	19911227	199428	
KR 9606193	B1	19960509	KR 9124339	A	19911226	199917	

Priority Applications (No Type Date): JP 90408063 A 19901227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2251937	A		21	G01B-011/00	
JP 4225537	A		4	H01L-021/52	
US 5307154	A		8	G01B-011/00	
GB 2251937	B			G01B-011/00	
KR 9606193	B1			H01L-021/66	

Abstract (Basic): GB 2251937 A
The chip position detector has a film table for carrying a detection subject of a transparent film for **semiconductor** chips, and a light source. Optical fibre cables have one end connected to the light source and the other end opened at a position under the film, to radiate a light beam onto the chips through the film. A position detector above the film recognises chip locations based on their shadow shapes on the film.
The film comprises polymers which do not interfere with the passage of light, and the film thickness is giverned by the material used, and the size and number of chips to be placed on it.
USE/ADVANTAGE - Precise position detection of chips partic. for those which vary in surface condition and are **die**-bonded e.g. LEDs.
Dwg.3/7
Abstract (Equivalent): GB 2251937 B
An apparatus for detecting the positions of **semiconductor** chips mounted on a transparent film, comprising: a film table for carrying said film; a light **source** provided on **one** side of the film table; an optical fibre cable for conveying light from said light source to illuminate the other side of said film table; first shutter means between the light source and the film table for selectively allowing illumination of the film table from said one side; second shutter means for selectively allowing illumination of the film table by way of said optical fibre cable from said other side; and detecting means provided for detecting the positions of the **semiconductor** chips from said one side.
Abstract (Equivalent): US 5307154 A
The detector comprises a device for carrying a transparent film upon which **semiconductor** chips are placed and a light source.

An optical fibre cable having one end connected to the light source and another end opened at a position on a second side of the transparent film radiates light beam from the optical fibre cable onto the **semiconductor** chips through the transparent film. A position recognition device is provided on a first side of the transparent film for recognizing positions of the **semiconductor** chips based on shadow shapes.

The light source is positioned above the film carrying device and provided with two shutter device, one of which is interposed between the light source and the optical fibre cable and another between the light source and the film carrying device, thereby radiating a light beam above and below the **semiconductor** chip in selective fashion.

USE/ADVANTAGE - Detecting positions of diced chips placed on film in case where they are **die** bonded to a **lead frame** by **die** bonding device, esp where chips are LEDs which vary in surface condition.

Dwg.3/7

32/3,AB/30 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008945077
WPI Acc No: 1992-072346/199209
XRPX Acc No: N92-054337

Insulated **lead frame** using plasma-sprayed dielectric - with layer of plasma spray ceramics below 125 microns thickness applied at lead ends and **die attach area**

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: DEVOS J W G; OMMEN D M; PALMER R H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5087962	A	19920211	US 91660206	A	19910225	199209	B

Priority Applications (No Type Date): US 91660206 A 19910225

Abstract (Basic): US 5087962 A

A **die attach area** is provided on a first surface of a **semiconductor** device **lead frame**. Leads project outward from the **die attach area**. The leads have proximal lead ends near the **die attach area**. A layer of plasma spray ceramic material is less than approximately 125 microns thick on a second surface of the **lead frame**. The layer of plasma sprayed ceramic material covers at least a portion of the proximal lead ends and an area that is opposite the **die attach area**.

The plasma sprayed ceramic material includes a plasma sprayed aluminium oxide filled ceramic material. A thin metallic layer is provided on the plasma sprayed ceramic material.

USE - Insulated **lead frame** for a **semiconductor** package providing high conductivity. (4pp Dwg.No.2/2)

32/3,AB/31 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008538956
WPI Acc No: 1991-043019/199106
XRPX Acc No: N91-033245
Semiconductor pressure difference sensor - comprises two pressure-sensing diaphragms attached to support frame formed by **cut lead frame**
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: TADA Y; TAKASHIMA A; YASUI K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4984466	A	19910115	US 90531428	A	19900531	199106	B

Priority Applications (No Type Date): JP 89U65133 U 19890602

Abstract (Basic): US 4984466 A
A **semiconductor** pressure sensor comprises two identical pressure sensing diaphragms, each having first and second pressure receiving surfaces and supported to align in a common plane in the same orientation. A housing includes at least two parts connected by a bonding agent to define fluid passages in communication with the pressure sensing diaphragms. An electrically conductive support frame holds the pressure sensing diaphragms and is embedded within the bonding agent between two parts of the housing.
The support frame includes a support plate portion and terminal portions having inner ends embedded within the bonding agent and outer ends projecting outwardly of the bonding agent for external connections. The support frame is formed by cutting a **lead frame** having a support frame portion and terminal portions along an outer contour of the housing except for the terminals.
USE - **Semiconductor** pressure sensor used for detecting a pressure difference between **two sources**. (5pp Dwg.No.1/3)

32/3,AB/32 (Item 31 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008174531
WPI Acc No: 1990-061532/199009
XRAM Acc No: C90-026695
XRPX Acc No: N90-047215
Semiconductor device prodn. - by forming **lead frame** and **attaching** upper and lower **gate** of **die**, for sealing **semiconductor** chips with resin
Patent Assignee: FUJI AUTOMATION KK (FUJI-N); FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2009142	A	19900112				199009	B

Priority Applications (No Type Date): JP 880 A 19880628; JP 88160198 A 19880628
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2009142	A		7		

Abstract (Basic): JP 2009142 A
Producing **semiconductor** device comprises forming **lead frame** with notched part and allowing upper and lower gates of a

die to communicate mutually when **lead frame** is set in **die.**

USE - For sealing **semiconductor** chips with resins with its **lead frame.**

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32/3,AB/33 (Item 32 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007359989
WPI Acc No: 1987-356995/198751
XRAM Acc No: C87-152786
XRPX Acc No: N87-267531
Thermal bonding appts. - using resistance heating elements with distributed mass to provide uniform heating
Patent Assignee: FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: CLARK J W; DRUMMOND F
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 250296	A	19871223	EP 87401304	A	19870611	198751	B
JP 63067740	A	19880326	JP 87150338	A	19870618	198818	
US 4804810	A	19890214	US 88170564	A	19880314	198909	
EP 250296	B1	19940209	EP 87401304	A	19870611	199406	
DE 3789034	G	19940324	DE 3789034	A	19870611	199413	
			EP 87401304	A	19870611		

Priority Applications (No Type Date): US 86876317 A 19860619
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 250296	A	E	9		
Designated States (Regional): DE FR GB IT NL					
US 4804810	A		8		
EP 250296	B1	E	11	H01L-021/00	
Designated States (Regional): DE FR GB IT NL					
DE 3789034	G			H01L-021/00	Based on patent EP 250296

Abstract (Basic): EP 250296 A

Bonding appts. has a thermally and electrically insulating frame (12) with at least two linear resistance heating elements (30) mounted thereon. Each element (30) has a distributed mass selected to provide even heating along its entire length when current is applied.

USE/ADVANTAGE - Particularly in the tape automated eutectic bonding of **semiconductor dies** to **lead frames** and other substrates. Eutectic bonding requires high degree of temp. uniformity to achieve reliable bonds. New tool provides precisely controlled temp. along the entire length of the heating element.

6/9

Abstract (Equivalent): EP 250296 B

A bonding apparatus (10) comprising: an elongated core (14) composed of an electrically and thermally insulating material, four electric power buses (20) arranged around said core (14) in a square array and mounted along said core (14), means for connecting the positive pole of a power **source** to a **first** diagonally opposed pair of said buses (20a) and a negative pole thereof to a second diagonally opposed pair of said buses (20b), thereby defining positive buses (20a) and negative buses (20b), four linear resistance heating elements (30), each of said elements including a pair of

electrically conductive legs (42) and a rail (40) extending between said legs (42), wherein one leg (42) of each pair is electrically connected to a positive bus (20a) and the other leg to a negative bus (20b), the lower end of each bus (20a, 20b) being connected to two elements (30), characterised in that said rail (40) has a variable cross-section area which is greatest at the middle of said rail (40) and continuously diminishes from the middle to said legs, such variable cross-section area providing substantially even heating along the entire length of each element (30) when current is applied.

Dwg.1/9

Abstract (Equivalent): US 4804810 A

Bonding equipment for interconnecting tape leads between **semiconductor dies** and **lead frames** or other substrates has a frame (12) of insulating material, consisting of a square core (14) with flange (16) and extension (18), with four electric power bus members (20a, 20b) mounted about its periphery. Buses are rectangular, with a chamfered face (22) mating against the flat surface of the core. Linear heating elements (30) are attached to the lower ends of the buses, such that a pair of diagonally opposed buses (20a) are coupled to a first L-shaped connector (32a), while the second pair of buses (20b) is connected to a second connector (32b). Connectors are attached to opposite poles of a power source.

ADVANTAGE - Highly uniform temp. control, with low thermal mass allowing rapid heating and cooling. (8pp

32/3,AB/34 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

03425442

MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 03-088342 [JP 3088342 A]
PUBLISHED: April 12, 1991 (19910412)
INVENTOR(s): SUGAWARA TAKEHISA
SUZUKI HIDEO
YAMAKAGE KAZUHIDE
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-223632 [JP 89223632]
FILED: August 31, 1989 (19890831)
JOURNAL: Section: E, Section No. 1086, Vol. 15, No. 265, Pg. 80, July 05, 1991 (19910705)

ABSTRACT

PURPOSE: To make it possible to ensure the reading of a silver paste pattern by obliquely projecting light on a **die** stage for a **lead frame** to which a **semiconductor** chip is bonded by using conductive paste in the direction along one side of the **semiconductor** chip so that a high contrast ratio is imparted between the **die** stage and the silver paste.

CONSTITUTION: Downward lighting is applied on a chip 2 which is mounted and bonded on a mat **die** stage 1 in the direction orthogonal to the **die** stage 1. A **second** light **source** 7 is provided so as to project light on the surface of the **die** stage 1 in the oblique direction. The light is projected in the direction orthogonal to the two facing sides of the chip 2. The illuminance of the surface of the **die** stage 1 becomes high because of the oblique lighting source 7. In the mean

time, the illuminance of the surface of a silver paste 3 at the two sides which are in parallel with the oblique lighting source 7 does not become high with respect to the surface of the silver paste 3. High contrast is obtained between the silver paste and the **die** stage 1. In this way, the direction of the slant projecting light is alternately switched, and the pattern of the silver paste 5 which is swelling out the peripheral part of the chip can be read out.

01077157
SEMICONDUCTOR DEVICE

PUB. NO.: 58-014557 [JP 58014557 A]
PUBLISHED: January 27, 1983 (19830127)
INVENTOR(s): SONO RIKURO
YURINO TAKAHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-111886 [JP 81111886]
FILED: July 17, 1981 (19810717)
JOURNAL: Section: E, Section No. 170, Vol. 07, No. 88, Pg. 45, April 12, 1983 (19830412)

ABSTRACT

PURPOSE: To obtain a dual-in-line package type IC which is free from cracks, by enlarging the size of a **die attaching** part of a **lead frame** and by providing through holes when a semicondutor chip **mounted** on the **die attaching** part is molded with resin.

CONSTITUTION: A **die attaching** part 2 provided in the central part of a **lead frame** 1 is prepared to be larger than a vonventional one, and a number of through holes 6 are bored therein. A **semiconductor** chip 3 is **mounted** on the **die attaching** part 2 thus constituted, terminals provided in the chip are bonded with lead terminals by lead wires 4, and then molding is made by using resin 5. By this method, the frame **area** of the **die attach** part 2 is reduced owing to the presence of the through holes 6, the differences in a thermal expansion coefficients of the frame, the chip and the resin from each other found after molding are thereby reduced, and thus the generatin of cracks are lessended remarkably.

39/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014358152
WPI Acc No: 2002-178853/200223
Related WPI Acc No: 1999-203963; 2000-557520; 2000-627920; 2002-054362; 2002-138236; 2002-163055; 2002-279757; 2002-291189; 2004-096661; 2004-096662; 2004-096663
XRAM Acc No: C02-055354
XRPX Acc No: N02-136008

Manufacture of plastic **lead frame** structure for **semiconductor** devices, involves forming plastic **lead frame** structure from polymeric material, and coating frame structure with conductive material

Patent Assignee: JIANG T (JIAN-I); KING J L (KING-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: JIANG T; KING J L
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010051397	A1	20011213	US 97878935	A	19970619	200223 B
			US 98195765	A	19981118	
			US 2000639359	A	20000814	
			US 2001921535	A	20010803	
US 6544820	B2	20030408	US 97878935	A	19970619	200327
			US 98195765	A	19981118	
			US 2000639359	A	20000814	
			US 2001921535	A	20010803	

Priority Applications (No Type Date): US 97878935 A 19970619; US 98195765 A 19981118; US 2000639359 A 20000814; US 2001921535 A 20010803
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010051397	A1		9	H01L-021/44	Cont of application US 97878935
					Cont of application US 98195765
					Cont of application US 2000639359
					Cont of patent US 5879965
					Cont of patent US 6124151
					Cont of patent US 6294410
US 6544820	B2			H01L-021/44	Cont of application US 97878935
					Cont of application US 98195765
					Cont of application US 2000639359
					Cont of patent US 5879965
					Cont of patent US 6124151
					Cont of patent US 6294410

Abstract (Basic): US 20010051397 A1
Abstract (Basic):

NOVELTY - The method involves forming a plastic **lead frame** (10) structure from polymeric material, and coating the frame structure with a conductive material.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(i) manufacture of one or more portions of a **semiconductor** device. The method involves forming one or more conductive plastic **lead frame** having **several lead** fingers (12), by stamping and/or **etching** a conductive **lead frame**. A **semiconductor** device having several bond pads (14), is attached to a portion of one or more conductive plastic **lead frame**. One or more bond pads are connected to at least one lead finger. One or

more portions of the **semiconductor** device and conductive plastic **lead frame**, are encapsulated; and

(ii) manufacture of circuit card. The method involves attaching one or more integrated circuit (IC) packages to a circuit card. One or more IC packages contain at least one conductive plastic **lead frame** formed by stamping and/or **etching**.

USE - The **lead frame** is used for packaging integrated circuits, and for manufacture of **semiconductor** devices and integrated circuits.

ADVANTAGE - Manufacturing cost of the plastic **lead frame** is reduced when compared with the manufacture of metal **lead frame**. Transparency, corrosion resistance and oxidation resistance of the plastic or composite plastic **lead frame**, are enhanced. The **lead frame** maintains its characteristics necessary for use in commercial production of IC packages. The overall cost of IC chip packaging is reduced by using plastic **lead frames** coated with conductive layers. The use of transparent polymers and intrinsically conductive polymers facilitates ultraviolet (UV) or other light **source** cure of **die attach** materials. The methods used to produce such **lead frames** are simple and can be easily incorporated into existing high-speed production lines for manufacturing IC chips.

DESCRIPTION OF DRAWING(S) - The figure shows the perspective view of the **lead frame**.

Plastic **lead frame** (10)

Lead fingers (12)

Bond pads (14)

pp; 9 DwgNo 3/7

41/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008778948
WPI Acc No: 1991-282965/199139
XRPX Acc No: N91-216414
Resin seal type **semiconductor** device - supplies power by connecting pads to supply via bonding lead and is sealed by mould resin
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KOMENAKA K
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 447922	A	19910925	EP 91103751	A	19910312	199139	B
JP 3263334	A	19911122	JP 9062037	A	19900313	199202	
US 5089879	A	19920218	US 91667335	A	19910311	199210	
EP 447922	B1	19951115	EP 91103751	A	19910312	199550	
DE 69114554	E	19951221	DE 614554	A	19910312	199605	
			EP 91103751	A	19910312		

Priority Applications (No Type Date): JP 9062037 A 19900313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 447922	A				
Designated States (Regional): DE FR GB					
EP 447922	B1	E	10	H01L-023/495	
Designated States (Regional): DE FR GB					
DE 69114554	E			H01L-023/495	Based on patent EP 447922

Abstract (Basic): EP 447922 A
The **semiconductor** device, of the resin seal type known as DIP (Dual In-line Package), supplying electric signals or potential to several isolated pads comprises a **lead frame** (21) with **die** support (33) carrying **several leads** (43) arranged on the underside. A **semiconductor** chip (51) with pads (52) connected to the leads (43) by bonding wires (10) is **mounted** on the **die** support (33) and a wire lead (46) coupled to the power source crosses above the chip and supplies power to at least two of the pads.
The whole device is sealed by mould resin (11).
ADVANTAGE - Reduced noise. (5pp Dwg.No.1/11

Abstract (Equivalent): EP 447922 B
A resin-sealed **semiconductor** device comprising: a **lead frame** (21) having a chip support (33) on the central portion of the **lead frame** (21) and a plurality of leads (43) arranged around the periphery of the chip support (33), each lead having a bonding site at its inner end adjacent to said chip support; a **semiconductor** chip (51) mounted on the chip support (33) and having a plurality of contact pads (52) on its surface respective ones of said contact pads (52) being wire bonded to respective ones of said bonding sites of said leads (43); and moulded resin (11) sealing the **lead frame** (21), the **semiconductor** chip (51), and the wire lead (46), characterised in that a further lead portion (46) of said **lead frame** is connected to one of said leads (43) and extends above and across said surface of said **semiconductor** chip (51) to a bonding post (45) adjacent to said chip support, said bonding post (45) being connected by a wire bond to a further one of said contact pads (52) of said chip (51).

Dwg.1/11

Abstract (Equivalent): US 5089879 A

The resin seal type **semiconductor** device comprises a **lead frame** having a support and a number of leads, a **semiconductor** chip **mounted** on the **die** support and having a number of pads connected to the leads. Furthermore, the device has a wire lead arranged above the **semiconductor** chip.

For example, power source is supplied from the lead supplying power **source** to **one** of the pads receiving power source, by connecting the lead and the **one** pad. Furthermore, power **source** is supplied from the lead to another pad located far from the one pad by connecting the lead and the another pad through the wire lead.

USE - DIP (Dual In-Line Package). (8pp

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015203794
WPI Acc No: 2003-264328/200326
XRAM Acc No: C03-069070
Up-set type exposed **lead-frame** package
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM C G; KIM H S; KIM S J; KWON Y A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002088270	A	20021127	KR 200127611	A	20010521	200326	B

Priority Applications (No Type Date): KR 200127611 A 20010521
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002088270	A		1	H01L-023/48	

Abstract (Basic): KR 2002088270 A
Abstract (Basic):

NOVELTY - An exposed **lead-frame** package(ELP) is provided to shorten the length of wire and reduce the wire loop height so that sweeping or tilting of a wire and the thickness of a package can be reduced by using up-set type lead produced by stamping method.

DETAILED DESCRIPTION - An ELP(100) includes a **semiconductor** chip and an inactive layer **attached** to a **die** pad(11) by glue(15). **Multiple** up-set type **leads**(103) around the **semiconductor** chip are connected to a bonding pad by wires(13). The height of up-set type leads is adjusted not to increase total thickness of the package. The distance between the bonding pad and wire is made shorter so that the length of wire is shortened and thus, wire loop height is also decreased. Wire sweeping and tilting phenomena are reduced thereby. The bottom surface of the **die** pad and lead is exposed and the **body** of package is formed by epoxy molding compound.

pp; 1 DwgNo 1/10

47/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014079827
WPI Acc No: 2001-564041/200163
Related WPI Acc No: 2002-223940
XRPX Acc No: N01-419824
Plastic **semiconductor** package for electronic assembly, has at least one volume equalizing paddle configured to equalize volume of molding compound on either side of centerline of package **body**
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: CORISIS D J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6229202	B1	20010508	US 2000480086	A	20000110	200163	B

Priority Applications (No Type Date): US 2000480086 A 20000110
Patent Details:

Patent No Kind Lan Pg   Main IPC   Filing Notes
US 6229202   B1   14 H01L-023/34

Abstract (Basic): US 6229202 B1
Abstract (Basic):
NOVELTY - The **semiconductor** package (16) includes a molded package **body** (18) comprising a molding compound encapsulating a **semiconductor die** (32) comprising a face and multiple bond pads (36) on the face. A **leadframe** segment (28S) is **attached** to the **die** and encapsulated in the package **body**. The **leadframe** segment comprises **multiple lead** fingers (30) attached to the face and wire bonded to the bond pads.

DETAILED DESCRIPTION - At least one volume equalizing paddle is configured to equalize a volume of the molding compound on either side of the centerline of the package **body**. An INDEPENDENT CLAIM is also included for an electronic assembly.

USE - For electronic assemblies, such as printed circuit boards and multi chip modules.

ADVANTAGE - Provides bow resistant plastic **semiconductor** package, thus improving construction of electronic assemblies, such as printed circuit boards and multi chip modules. Eliminates stresses on bonded connections between package leads and electrodes on a substrate of assembly due to planarity of package leads.

DESCRIPTION OF DRAWING(S) - The figure is an enlarged cross-sectional view of the **semiconductor** package.

Semiconductor package (16)
Package **body** (18)
Leadframe segment (28S)
Lead fingers (30)
Semiconductor die (32)
Bond pads (36)
pp; 14 DwgNo 2E/5

47/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011806178
WPI Acc No: 1998-223088/199820
XRPX Acc No: N98-176944
Lead frame for **semiconductor** chip mounting - has offset member which gives difference in elevation positions of **die** pad and leads
Patent Assignee: HITACHI CHO LSI ENG KK (HISC); HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 10065089 A 19980306 JP 96213595 A 19960813 199820 B

Priority Applications (No Type Date): JP 96213595 A 19960813
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 10065089 A 8 H01L-023/50

Abstract (Basic): JP 10065089 A
The **lead frame** has **multiple leads** which are electrically connected to a **semiconductor** chip. A **die** pad **mounts** the **semiconductor** chip.

A tab suspension lead (7) **couples** the **die** pad and the main **body**. An offset member (9) which includes a flat portion (9a) in- between two ramp portions (9b1,9b2), gives difference in elevation positions of the **die** pad and the leads.

ADVANTAGE - Obtains huge quantity of offset. Obtains favourable quality. Prevents bending of **semiconductor** device due to thermal stress.

Dwg.2/9

47/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011713059
WPI Acc No: 1998-129969/199812
XRPX Acc No: N98-102619

Flagless **semiconductor** device - has **lead frame** with tie bars extending into **die** receiving area which act as sole support for **semiconductor die**, edges of tie bars form space filled by no other **lead frame** part

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: PRZANO M C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5714792	A	19980203	US 94315545	A	19940930	199812	B

Priority Applications (No Type Date): US 94315545 A 19940930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5714792	A		8	H01L-023/495	

Abstract (Basic): US 5714792 A

The flagless **semiconductor** device (10) includes a flagless **leadframe** (13) which has **several leads** (16) with inner and outer lead portions. The inner lead portions define a **die** receiving area. Exactly two tie bars (20) extend into the **die** receiving area from two opposing sides without overlapping. Each tie bar has a straight stem (22) for physical connection to a handling rail (12) and a support (24) extending from the straight stem. Each tie bar is straight and each support terminates at an edge.

The edges face each other to form a space that is unoccupied by any other **leadframe** part. The support is the same width as the straight stem. A **semiconductor die** (11) has two opposing edges and a centre. The edges of the **die** are **attached** to the supports of the tie bars so that the centre of the **semiconductor die** spans the space between them and is not supported by any other part of the **leadframe**. The **semiconductor die** is electrically **connected** to the inner portions of the leads. A package **body** encapsulates the **semiconductor die** and the inner lead portions of the leads.

ADVANTAGE - Eliminates delamination of external encapsulant from **lead frame** flag. Allows **lead frame** to be used with several different **die** sizes.

Dwg.1/6

47/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011572518
WPI Acc No: 1997-548999/199750
XRPX Acc No: N97-457806
Thermally enhanced **lead frame** manufacturing method for **semiconductor** device package - locating inner section of leads on first plane co-planar with thermal fin, with X-shaped **die** support positioned in central cavity on second plane
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: JOINER B A; RIDSDALE G L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5683944	A	19971104	US 95522889	A	19950901	199750	B

Priority Applications (No Type Date): US 95522889 A 19950901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5683944	A		7	H01L-021/58	

Abstract (Basic): US 5683944 A
The method includes the provision of a copper **lead frame** (10) that has **many leads**, having both inner (20) and outer sections, arranged around a central cavity, and several tie bars (16) attached to which is an X-shaped **die** support (12) structure. Onto the **die** support is **mounted** a **semiconductor die** (18) with wire bonding **linking** the **die** to the inner section of the leads, and around the **die**, the wire bonds, the lead inner sections and the thermal bars is formed a package **body**.
The lead inner sections are located on a first plane with the **die** support positioned in the central cavity on a second plane. To one of the bars is attached a thermal fin that is substantially co-planar with the leads. The **die** is positioned in the cavity such that the fin lies between a **die** edge and the inner section of the leads, and it does not overlie or contact the fin.
USE/ADVANTAGE - For high input/output count microprocessor and ASIC. Good package cracking and delamination performance with enhanced thermal dissipation.
Dwg.2/5

47/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011499546
WPI Acc No: 1997-477459/199744
XRAM Acc No: C97-151664
XRPX Acc No: N97-398243
Lead frame for mounting resin seal **semiconductor** device - has insulator whose thickness is set larger than that of plating thickness of plating areas of inner leads
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9223772	A	19970826	JP 9628815	A	19960216	199744	B

Priority Applications (No Type Date): JP 9628815 A 19960216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9223772	A		5	H01L-023/50	

Abstract (Basic): JP 9223772 A

The **lead frame** (1) has **multiple** inner **leads** (13) and a main **body** (11) which consists of a **die** pad (14) for **mounting** a **semiconductor** device. An insulator (18) is set up continuously at the end side of the **die** pad along the hoop direction. The inner **leads** have **multiple** plating areas (17). Plating of the plating area is performed with an electrically conductive material from the rear end side of the insulator. The thickness of the insulator is set greater than that of the plating thickness.

ADVANTAGE - **Semiconductor** devices of different kinds and sizes can be mounted. Manufacture of **semiconductor** device is simplified and costs are reduced. Electrical reliability of device is improved.

Dwg.1/5

47/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011372352
WPI Acc No: 1997-350259/199732
Related WPI Acc No: 1996-267908
XRPX Acc No: N97-290357

Semiconductor device packaging method for **leadframe** based package having external lead - patterning **leadframe** with indented tab from conductive foil, **mounting die** to **leadframe** centre and connecting it to lead inner portion, forming package around **die** and **body**, and extending tab of **leadframe** beyond periphery of package

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: CHIA C J; LIM S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5643835	A	19970701	US 92992643	A	19921218	199732	B
			US 94340727	A	19941116		
			US 96602896	A	19960216		

Priority Applications (No Type Date): US 92992643 A 19921218; US 94340727 A 19941116; US 96602896 A 19960216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5643835	A		10		Div ex application US 92992643 Cont of application US 94340727

Abstract (Basic): US 5643835 A

The method involves initially patterning a **leadframe** from a conductive foil, the **leadframe** having **several leads** and at least one tab element having a fixed coplanar relationship with the leads. This tab has dimpled hollow on one surface and a corresponding convex indentation (324) on the other for aligning the one tab with a planar substrate. A **die** is then **mounted** to a

central portion of the **leadframe** and the **die** is **connected** to inner portions of the leads.

A package **body** is then formed around the **die** and the central portion of the **leadframe**, outer portions of the leads extending beyond a periphery of the package **body**. The tab is then extended beyond the **body** periphery and proximate to it, the tab remaining in the fixed coplanar relationship with the outer portions of the leads.

USE/ADVANTAGE - For aligning lead of DIP, PQFP or PLCC, with trace of PWB. Tabs ensure accurate alignment of lead ends to socket contacts of test socket; and alignment of leads and PWB conductive traces. Using tabs for alignment of package in shipping trays, leads will not contact tray. Eliminates potential sources of lead damage, increasing effective yield and lowering costs.

2a,2b,7/7

47/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010770954
WPI Acc No: 1996-267908/199627
Related WPI Acc No: 1997-350259
XRPX Acc No: N96-225232

Packaged **semiconductor** device for printed wiring board - has tab dimple as part of **leadframe** tab which remains in fixed positional relationship with lead outer portions to align tabs with planar substrate

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: CHIA C J; LIM S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5521427	A	19960528	US 92992643	A	19921218	199627	B
			US 94340807	A	19941117		

Priority Applications (No Type Date): US 92992643 A 19921218; US 94340807 A 19941117
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5521427	A		11		Cont of application US 92992643

Abstract (Basic): US 5521427 A

The **semiconductor** device includes a **leadframe** patterned from a conductive foil, a **die**, and a package **body** formed around the **die**. The **lead frame** has **several leads** and at least one tab element in a positionally fixed coplanar relationship with the leads. The tab element has a concave positioning tab ''dimple'' on one surface and a corresponding convex positioning tab ''dimple'' on another surface. These ''dimples'' align the tab elements with a planar substrate.

The **die** is **mounted** to a central portion of the **leadframe** and is connected to inner portions of the leads. The package **body** is formed around the **die** and the central portion of the **leadframe**. The outer portions of the leads extend beyond a package **body** periphery. The tab elements extend beyond the **body** periphery and approximate to it, where the tab remains in a fixed positional relationship with the lead outer portions.

ADVANTAGE - Ensures accurate alignment of plastic packaged **semiconductor** devices to PWB or other mountable media having wiring patterns. Modification of mould set is not required. Inter-lead

distance is not limited. Min. spacing is in order of 0.25mm or less.
Dwg.2b,7/7

47/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009702874
WPI Acc No: 1993-396427/199350
XRPX Acc No: N93-306396
Semiconductor device with lead-on-chip-structure - has brazing solder material with no moisture absorption, formed on surface of **semiconductor** component and fixed to support plate
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI ELECTRIC KK (MITQ)
Inventor: ABE S; ICHIYAMA H; NISHINAKA Y; TOMITA Y; UEDA N
Number of Countries: 004 Number of Patents: 017
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4318727	A1	19931209	DE 4318727	A	19930604	199350	B
JP 5343445	A	19931224	JP 92145697	A	19920605	199405	
DE 4345302	A1	19950803	DE 4318727	A	19930604	199536	
			DE 4345302	A	19930604		
DE 4345305	A1	19950803	DE 4318727	A	19930604	199536	
			DE 4345305	A	19930604		
DE 4345301	A1	19950810	DE 4318727	A	19930604	199537	
			DE 4345301	A	19930604		
DE 4345303	A1	19950810	DE 4318727	A	19930604	199537	
			DE 4345303	A	19930604		
US 5535509	A	19960716	US 9370990	A	19930604	199634	
			US 94325637	A	19941019		
DE 4318727	C2	19980312	DE 4318727	A	19930604	199814	
US 5724726	A	19980310	US 9370990	A	19930604	199817	
			US 94325637	A	19941019		
			US 96614552	A	19960313		
DE 4345305	C2	19980409	DE 4318727	A	19930604	199818	
			DE 4345305	A	19930604		
US 5763829	A	19980609	US 9370990	A	19930604	199830	
			US 94325637	A	19941019		
			US 95506852	A	19950725		
US 5900582	A	19990504	US 9370990	A	19930604	199925	
			US 94325637	A	19941019		
			US 95506852	A	19950725		
			US 9850397	A	19980331		
KR 9703912	B1	19970322	KR 9310135	A	19930604	199937	
JP 3088193	B2	20000918	JP 92145697	A	19920605	200048	
DE 4345301	C2	20031120	DE 4318727	A	19930604	200378	
			DE 4345301	A	19930604		
DE 4345303	C2	20031204	DE 4318727	A	19930604	200381	
			DE 4345303	A	19930604		
DE 4345302	C2	20031211	DE 4318727	A	19930604	200401	
			DE 4345302	A	19930604		

Priority Applications (No Type Date): JP 92145697 A 19920605; ES 921158 A 19920604; ES 93928 A 19930503
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4318727	A1		48	H01L-023/50	
JP 5343445	A			H01L-021/52	

DE 4345302	A1	1	H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
DE 4345305	A1	1	H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
DE 4345301	A1		H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
DE 4345303	A1		H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
US 5535509	A	37	H01R-043/00	Div ex application US 9370990
DE 4318727	C2	19	H01L-023/50	Div in patent DE 4345301
				Div in patent DE 4345302
				Div in patent DE 4345303
				Div in patent DE 4345305
US 5724726	A	36	H01R-043/00	Div ex application US 9370990
				Div ex application US 94325637
				Div ex patent US 5535509
DE 4345305	C2	13	H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
US 5763829	A		H01L-023/02	Div ex application US 9370990
				Div ex application US 94325637
				Div ex patent US 5535509
US 5900582	A		H01L-023/28	Div ex application US 9370990
				Div ex application US 94325637
				Cont of application US 95506852
				Div ex patent US 5535509
				Cont of patent US 5763829
KR 9703912	B1		H01L-023/50	
JP 3088193	B2	21	H01L-021/52	Previous Publ. patent JP 5343445
DE 4345301	C2		H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
DE 4345303	C2		H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727
DE 4345302	C2		H01L-023/50	Div ex application DE 4318727
				Div ex patent DE 4318727

Abstract (Basic): DE 4318727 A

The device includes a **semiconductor** component (2) having electrodes (4) formed on one of a pair of surfaces, and supported by a support plate (1). A brazing solder with no moisture absorption is formed on the other surface and is fixed to the support plate.

Multiple leads (3) have an inner section, which extends above the **semiconductor** component, and a connected outer section, which extends outside the component. The inner sections of the leads are connected to corresponding electrodes by thin metal wires (5). The above parts are sealed in a housing (6) with the outer sections of the leads extending outwards. A **lead frame** is also claimed.

ADVANTAGE - No corrosion problems occur in device. Prevents moisture being given off during mfr.

Dwg.1/35

Abstract (Equivalent): US 5724726 A

The device includes a **semiconductor** component (2) having electrodes (4) formed on one of a pair of surfaces, and supported by a support plate (1). A brazing solder with no moisture absorption is formed on the other surface and is fixed to the support plate.

Multiple leads (3) have an inner section, which extends above the **semiconductor** component, and a connected outer section, which extends outside the component. The inner sections of the leads are connected to corresponding electrodes by thin metal wires (5). The above parts are sealed in a housing (6) with the outer sections of the leads extending outwards. A **lead frame** is also claimed.

ADVANTAGE - No corrosion problems occur in device. Prevents

moisture being given off during mfr.
Dwg.1b/35
US 5535509 A
A method for producing a **semiconductor** device having a lead on chip (LOC) structure using a first frame including an outer frame in a first plane and a **die** pad **connected** to the outer frame and displaced from the first plane, and a second frame comprising an outer **lead frame**, a plurality of leads extending inwardly from the outer **lead frame**, and frame-cutting slits in said outer **lead frame** of said second frame for cutting a portion of said first frame after said second frame is connected to said first frame, said method comprising, sequentially:
die-bonding a **semiconductor** chip to said **die** pad of said first frame;
connecting said second frame to said first frame with an inner lead portion of each of said leads extending across said **semiconductor** chip **mounted** on said **die** pad and with the slits in said second frame exposing parts of said outer frame of said first frame;
cutting said exposed parts of said outer frame of said first frame at the frame-cutting slits of said second frame and removing said exposed parts of said outer frame of said first frame, leaving a remaining part of said first frame including said **die** pad **connected** to said second frame;
wire-bonding wires between said **semiconductor** chip and said inner lead portions of said leads;
encapsulating said **semiconductor** chip, said remaining part of said first frame including said **die** pad, said wires, and parts of said second frame in a resin **body** with an outer lead portion of each of said leads exposed outside of said resin **body**;
plating said outer lead portions exposed outside of said resin **body**;
cutting said outer **lead frame** of said second frame exposed outside of said resin **body** to separate said outer lead portions from each other; and
deforming each of said outer lead portions exposed outside of said resin **body** into a desired shape.
Dwg.2,5/35

47/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009182428
WPI Acc No: 1992-309864/199238
XRPX Acc No: N92-237197
Lead frame and resin sealed **semiconductor** circuit for protection - has bars connected to **body** with mounting pad connected to bars and **multiple leads** extending to pad comprising multiple dimples formed by pushing material
Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE)
Inventor: NOSE S
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 503769	A1	19920916	EP 92301150	A	19920212	199238	B
JP 5055430	A	19930305	JP 9222304	A	19920207	199314	
US 5397915	A	19950314	US 92834466	A	19920212	199516	
EP 503769	B1	19981223	EP 92301150	A	19920212	199904	
DE 69227937	E	19990204	DE 627937	A	19920212	199911	

				EP 92301150	A	19920212	
JP 3040235	B2	20000515	JP 9222304		A	19920207	200028

Priority Applications (No Type Date): JP 9118168 A 19910212
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 503769	A1	E	13	H01L-023/495	
Designated States (Regional): DE FR GB					
JP 3040235	B2		9	H01L-023/50	Previous Publ. patent JP 5055430
US 5397915	A		11	H01L-023/48	
EP 503769	B1	E		H01L-023/495	
Designated States (Regional): DE FR GB					
DE 69227937	E			H01L-023/495	Based on patent EP 503769
JP 5055430	A			H01L-023/50	

Abstract (Basic): EP 503769 A
Lead frame comprises the bars (16) connected to **body** (12a, 12b) with a **semiconductor** element monting **die** pad (14) **connected** to the bars with **multiple leads** (15) extending to **mounting die** pad. Dam bar (17) is connected to **leads** (15) characterised by **multiple** slits (18) and dimples (19) are disposed in **mounting die** pad. Dimples are formed by pushing out material of pad adjacent slits.
Dimples (19) form symmetrical pattern about a point. Leads are connected to element through metal wires (20) with resin mold portion (21) enveloping element (13) and **mounting die** pad (14).
ADVANTAGE - Gives sufficient mechanical strength preventing destruction during soldering.
Dwg.2/11
Abstract (Equivalent): US 5397915 A
A **semiconductor** element **mounting die** pad is supported by tie bars. Slits and dimples are disposed on a flat surface. The slits penetrate from the face to the back side of the **semiconductor** element **mounting die** pad. Slits are formed, e.g. by a punching or chemical **etching** method. These forming methods are the same as the method of forming the **lead frame**. Accordingly, if slits are disposed simultaneously when forming the **lead frame**, the process is not complicated.
Slits of the same shape are formed at an interval of the width of dimples. The rear side is pushed out to form dimples with the boundary of the slits. Thus, slits are formed in one **body** at both ends of the dimples. By thus composing, the thin type surface mount **semiconductor** device has a sufficient mechanical strength, and is capable of controlling the stress in a narrow region so that a **semiconductor** device of high reliability is realized.
Dwg.1/11

47/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009028641
WPI Acc No: 1992-156001/199219
XRPX Acc No: N93-180763
Semiconductor device with noise reducing **die** pads - has **semiconductor** chip, **lead@ frame** composed of **die** pad, **several leads** and sealed **body** made by resin moulding the chip and frame
Patent Assignee: TOSHIBA KK (TOKE); TOSHIBA MICROELECTRONICS CORP (TOSZ

)
Inventor: KOZUKA E
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 4094565	A	19920326	JP 90213050	A	19900810	199219	B
US 5229846	A	19930720	US 91746026	A	19910812	199330	

Priority Applications (No Type Date): JP 90213050 A 19900810
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 4094565	A		7		
US 5229846	A		14	H01L-023/02	

Abstract (Basic): JP 4094565 A
The **semiconductor** device includes a **semiconductor** chip, a **lead frame** composed of a **die** pad for **mounting** the **semiconductor** chip thereon and a number of leads each having one end located near the **die** pad and its other end located outside of a package. A sealed **body** is made by resin moulding the **semiconductor** chip and the **lead frame** except the other end of each lead, wherein the **die** pad is divided into a number of small pieces. At least one of the divided pieces is electrically connected to at least one of the leads to which a predetermined potential is applied. The size of each of the small pieces is different from each other, and a larger piece is connected to a lead on which noise is likely to be generated.
ADVANTAGE - Reduced inductance and resistance components of voltage supply lines within chip to eliminate noise.
US 5229846 A
The **semiconductor** device includes a **semiconductor** chip, a **lead frame** composed of a **die** pad for **mounting** the **semiconductor** chip thereon and a number of leads each having one end located near the **die** pad and its other end located outside of a package. A sealed **body** is made by resin moulding the **semiconductor** chip and the **lead frame** except the other end of each lead, wherein the **die** pad is divided into a number of small pieces. At least one of the divided pieces is electrically connected to at least one of the leads to which a predetermined potential is applied. The size of each of the small pieces is different from each other, and a larger piece is connected to a lead on which noise is likely to be generated.
ADVANTAGE - Reduced inductance and resistance components of voltage supply lines within chip to eliminate noise.
Dwg.1/13
Abstract (Equivalent): US 5229846 A
The **semiconductor** device includes a **semiconductor** chip, a **lead frame** composed of a **die** pad for **mounting** the **semiconductor** chip thereon and a number of leads each having one end located near the **die** pad and its other end located outside of a package. A sealed **body** is made by resin moulding the **semiconductor** chip and the **lead frame** except the other end of each lead, wherein the **die** pad is divided into a number of small pieces. At least one of the divided pieces is electrically connected to at least one of the leads to which a predetermined potential is applied. The size of each of the small pieces is different from each other, and a larger piece is connected to a lead on which noise is likely to be generated.
ADVANTAGE - Reduced inductance and resistance components of voltage supply lines within chip to eliminate noise.

(Dwg.1/13

47/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008540262
WPI Acc No: 1991-044325/199106
XRPX Acc No: N91-034385
Lead frame system with **multi**-tier **leads** -
includes **die attach** pad and leads with tips in vicinity of
pad and alternate lead tips bent upwards into on plane
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N); VLSI TECH INC (VLSI-N)
Inventor: JOHNSON D P
Number of Countries: 015 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4987473	A	19910122	US 89389038	A	19890803	199106	B
WO 9102378	A	19910221				199110	
JP 5501176	W	19930304	JP 90510985	A	19900627	199314	
			WO 90US3624	A	19900627		

Priority Applications (No Type Date): US 89389038 A 19890803
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9102378	A				
Designated States (National): JP KR					
Designated States (Regional): AT BE CH DE DK ES FR GB IT LU NL SE					
JP 5501176	W			H01L-023/50	Based on patent WO 9102378

Abstract (Basic): US 4987473 A
A unitary **lead frame** includes a **die attach** pad and leads with lead tips in the vicinity of the pad. The leads are an integral part of the unitary **lead frame**. The lead tips are electrically connected to selected points on the **die**, the tips being in two or more different planes. A **body** encloses the **lead frame**, the **die** and the **connector** to fix the positions of the **lead frame** and the conntor relative to the **die**.
The leads are so located relative to the **die attach** pad that when the **die** is supported by the **die attach** pad, and when the **die**, the leads an **connector** are fixed in position by the **body**, the tips of the leads ae spaced apart from the **die**. The distance between the lead tips is less than about 500 mils. The lead tips are in two different planes.
USE - Package for holding a **semiconductor die** of a predetermined size esp. for VLSI use.
Dwg.6/6

47/3,AB/13 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05193124
MANUFACTURE OF **SEMICONDUCTOR** DEVICE AND **SEMICONDUCTOR** DEVICE AND **LEAD FRAME**

PUB. NO.: 08-148624 [JP 8148624 A]

PUBLISHED: June 07, 1996 (19960607)
INVENTOR(s): TADA NOBUHIKO
OGATA KOJIRO
UNO YOSHIYUKI
APPLICANT(s): HITACHI CONSTR MACH CO LTD [351479] (A Japanese Company or Corporation), JP (Japan)
UNO YOSHIYUKI [000000] (An Individual), JP (Japan)
APPL. NO.: 06-282291 [JP 94282291]
FILED: November 16, 1994 (19941116)

ABSTRACT

PURPOSE: To obtain a high-quality product without being affected by dross in a **semiconductor** device, which permits bending and forming for outer leads and cutting for dam bars while maintaining highly accurate shapes for narrow- pitch and **multi**-pin **lead frames**.

CONSTITUTION: After sealing a **semiconductor** chip and **lead frame** as a united **body** with resin molding, outer leads 3 coupled with a dam bar 4 and a coupling portion 5 are bent and formed as an united **body** . At this time, an outer frame portion 7 is fixed and smoothly bent and formed by utilizing elongation deformation of a deforming portion 6 provided between the coupling portion 5 and the outer frame portion 7. Next, dam bars 4 are **cut** by laser, and dross generated is almost fully removed by a chemical treatment. Thereafter, solder plating is performed for the outer lead 3 and the **coupling** portion 5 is **cut** off.

47/3,AB/14 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01186347
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 58-123747 [JP 58123747 A]
PUBLISHED: July 23, 1983 (19830723)
INVENTOR(s): SUZUMURA YOSHIKAZU
YAMAZAKI ISAMU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI TOKYO ELECTRONICS CO LTD [464698] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-005922 [JP 825922]
FILED: January 20, 1982 (19820120)
JOURNAL: Section: E, Section No. 204, Vol. 07, No. 233, Pg. 165, October 15, 1983 (19831015)

ABSTRACT

PURPOSE: To improve the precision of lead bonding position by a method wherein a **leadframe** connected to a connector as one **body** is fixed to a base and then the **connector** is **cut** off.

CONSTITUTION: A **leadframe** 12 is formed of **several leads** 13 bent after punched in thin plate etc. The leads 13 comprise inner leads 14 and outer leads 15 while the inner leads 14 are connected to the connector 16 as one **body**. The frame 12 formed so far adheres to a base 10 making use of low melting point glass 18. Finally the **connector** 16 is **cut** off by means of laser beams and the like.

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  20apr04 10:17:05 User267149 Session D1346.1

File 342:Derwent Patents Citation Indx 1978-04/200420
       (c) 2004 Thomson Derwent
      1  PN=US 5789803
? MAP PN/CT=
? MAP PN/CG=
? MAP PN

SYSTEM:OS  - DIALOG OneSearch
  File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200425
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
```

Set	Items	Description
S1	47	S1:S7
S2	37	S1 AND SEMICONDUCT?
S3	16	S2 AND (LEADFRAM? OR LEAD()FRAM?)
S4	7	S3 AND (DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP OR ETCH???????? OR CUT OR TRIM?)
S5	9	S3 NOT S4
S6	9	IDPAT (sorted in duplicate/non-duplicate order)
S7	7	IDPAT (primary/non-duplicate records only)
S8	7	IDPAT S4 (sorted in duplicate/non-duplicate order)
S9	7	IDPAT S4 (primary/non-duplicate records only)

?

4/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015194273
WPI Acc No: 2003-254807/**200325**
Related WPI Acc No: 2003-362032
XRPX Acc No: N03-202022
Leaded **semiconductor** package used in portable electronic device, includes support bars and leads extending transversely from dam bars of panel to support several **lead frames** on panel
Patent Assignee: ST ASSEMBLY TEST SERVICES LTD (STAS-N)
Inventor: YEE J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6483177	B1	20021119	US 2000705251	A	20001102	200325	B

Priority Applications (No Type Date): SG 20005737 A 20001009
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6483177	B1		15	H01L-023/495	

Abstract (Basic): **US 6483177** B1
Abstract (Basic):
NOVELTY - The **semiconductor dies** are mounted to the **lead frames** (22a,22b) in a panel (70). The mounting paddles (72) connected between the opposite **lead frame** strips, are interconnected by the tie bars (74). The panel has a peripheral frame within which support bars (32a,32b) and leads (30a,30b) extend transversely from the dam bars (28a,28b).
USE - Leaded **semiconductor** package used in portable electronic device.
ADVANTAGE - Leaded **semiconductor** packages are easier to test, handle and transport, when connected together in the panel. Concept of punching and saw singulation allows higher throughput in forming leaded **semiconductor** packages as well as minimizing cost for each package. The support base serves to stiffen the panel against stress that is typically encountered during sawing.
DESCRIPTION OF DRAWING(S) - The figures show an enlarged view of a portion of the panel showing two **lead frames** and the plan view of a portion of the panel.
Lead frames (22a,22b)
Dam bars (28a,28b)
Leads (30a,30b)
Support bars (32a,32b)
Panel (70)
Mounting paddles (72)
Tie bars (74)
pp; 15 DwgNo 4, 6/11

4/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014582507
WPI Acc No: 2002-403211/200243
Related WPI Acc No: 2002-574770
XRPX Acc No: N02-316325

Dual leads-over-chip **semiconductor die** assembly for **semiconductor** package, has two **semiconductor dice** mounted back to back on either sides of base **lead frame**

Patent Assignee: VAIYAPURI V (VAIY-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: VAIYAPURI V
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020027271	A1	20020307	US 2001767446	A	20010123	200243	B
US 6541846	B2	20030401	US 2001767446	A	20010123	200324	

Priority Applications (No Type Date): SG 20005005 A 20000901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020027271	A1		14	H01L-023/495	
US 6541846	B2			H01L-023/495	

Abstract (Basic): US 20020027271 A1
Abstract (Basic):

NOVELTY - The **semiconductor dice** (120,130) are respectively attached on either sides of a **die** attachment site (116) of a base **lead frame**. Bond pads of the respective **semiconductor dice** are elastically connected to offset **lead frame** lead fingers wire bonded to primary lead fingers of the base **lead frame**.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) **Semiconductor die** assembly fabrication method;

(b) **Semiconductor** assembly

USE - Dual leads-over-chip (LOC) **semiconductor die** assembly having memory **dice**, for **semiconductor** integrated circuit (IC) package.

ADVANTAGE - Since two **semiconductor dice** are mounted on a common base **lead frame**, overall height of the stacked dual LOC **semiconductor die** assembly is minimized, thereby increases the packaging density of the integrated circuit. Also reduces the cause for electrical short circuiting between the **dice** of the assembly, as the active surfaces of the **die** are facing outwardly in opposite direction, hence reduces the damage to the **die** assembly.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the dual LOC **semiconductor die** assembly.

Die attachment site (116)

Semiconductor dice (120,130)

pp; 14 DwgNo 2/5

4/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014212411
WPI Acc No: 2002-033108/**200204**
Related WPI Acc No: 1998-119394; 2004-068193
XRAM Acc No: C02-009145
XRPX Acc No: N02-025439

Fabrication of **semiconductor** components, e.g. ball grid array packages, involves cutting decals from ribbons of adhesive tape and attaching **semiconductor dies** to substrates using the decals

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: VANNORTWICK J

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6281044	B1	20010828	US 95509048	A	19950731	200204 B
			US 9833497	A	19980302	
			US 99356267	A	19990716	

Priority Applications (No Type Date): US 99356267 A 19990716; US 95509048 A 19950731; US 9833497 A 19980302
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6281044	B1		17	H01L-021/58	Cont of application US 95509048
					CIP of application US 9833497
					CIP of patent US 6025212

Abstract (Basic): **US 6281044** B1
Abstract (Basic):

NOVELTY - A **semiconductor** component is fabricated by cutting decals from ribbons of adhesive tape, and then attaching a **semiconductor die** to a substrate using the decals.

DETAILED DESCRIPTION - Fabrication of a **semiconductor** component comprises:

(a) providing a **semiconductor die** (10);

(b) providing a substrate (14) comprising a polymer material;

(c) providing an adhesive tape of a predetermined width;

(d) providing a tape cutter apparatus for forming decals (52) with a first finished dimension equal to the width of the tape, and a second finished dimension equal to an indexed length of the tape;

(e) forming the decal using the tape cutter apparatus;

(f) attaching the decal to the substrate; and

(g) attaching the **die** to the substrate using the decals.

USE - For fabricating **semiconductor** components, e.g. ball grid array package or multi chip module (claimed).

ADVANTAGE - The invention makes decals without wasted tape, and with accurate alignment of the decal, the substrate, and the **die** to one another.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of a ball grid array package.

Semiconductor die (10)

Substrate (14)

Decals (52)

pp; 17 DwgNo 2c/8

4/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013717047
WPI Acc No: 2001-201271/**200120**
Related WPI Acc No: 2000-105105
XRPX Acc No: N01-143377

Semiconductor package manufacturing method involves disposing gap increasing layer between adhesive layer and **lead frame** to reduce trap of package particles in the gap between **semiconductor die** and **lead frame**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: KINSMAN L D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6133068	A	20001017	US 97944743	A	19971006	200120 B
			US 99264353	A	19990308	

Priority Applications (No Type Date): US 97944743 A 19971006; US 99264353 A 19990308

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6133068	A		9	H01L-021/50	Div ex application US 97944743 Div ex patent US 6005286

Abstract (Basic): **US 6133068** A

Abstract (Basic):

NOVELTY - An adhesive layer (114) is interposed between a **semiconductor die** (102) and a **lead frame**, such that a gap is defined by surfaces of **die**, **lead frame** and edge of adhesive layer. A gap increasing layer (200) of thickness 300 micro inches or more is disposed between the adhesive layer and **lead frame** for reducing trap of package particles in the gap.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor** device fabricating method.

USE - For manufacture of **semiconductor** package.

ADVANTAGE - Reduces stress to **die** surface by increasing the gap between **die** and **lead frame**. No extra cost is added to manufacturing process.

DESCRIPTION OF DRAWING(S) - The figure shows the enlarged cross-sectional diagram of packaged **semiconductor** device.

Semiconductor die (102)

Adhesive layer (114)

Gap increasing layer (200)

pp; 9 DwgNo 4A/6

4/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012933258

WPI Acc No: 2000-105105/**200009**

Related WPI Acc No: 1992-331732; 1995-022464; 1996-230601; 1998-052245; 2001-201993

XRAM Acc No: C00-031449

XRPX Acc No: N00-080732

Semiconductor assembly with a **die** surface bonded to a **lead frame**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: KINSMAN L D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6005286	A	19991221	US 97944743	A	19971006	200009 B

Priority Applications (No Type Date): US 97944743 A 19971006

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6005286	A		9	H01L-023/495	

Abstract (Basic): **US 6005286** A

Abstract (Basic):

NOVELTY - A **semiconductor** assembly with a **die** surface bonded to a **lead frame** includes a spacer layer between **die** surface and **lead frame** to increase the gap size and reduce the formation of trapped particles.

DETAILED DESCRIPTION - The **lead frame** is bonded to the **die** surface via an adhesive layer which does not extend to the edge of the **die**. The spacer layer neither extends to the edge of the **die** but increases the gap size and prevents particles being trapped between the edges of the **die** and the lead ends or lead fingers located over the **die** edges.

USE - Especially in forming an assembly which includes a leads-over-chip **die**.

ADVANTAGE - The assembly reduces the likelihood of trapped particles between **lead frame** and **die** surface which induce stress or damage etc., without need to modify the **lead frame** design.

DESCRIPTION OF DRAWING(S) - The drawings show the **die** assembly of the invention.

Semiconductor die (102)
Lead fingers (112)
Adhesive layer (114)
Spacer layer (200)
Boundary of adhesive layer (138)
Boundary of spacer layer (202)
Small filler particle which avoids entrapment in the gap between the lead finger and the **die** surface (130)
pp; 9 DwgNo 4A,B/6

4/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009777423
WPI Acc No: 1994-057275/**199407**
XRAM Acc No: C94-025769
XRPX Acc No: N94-045071

Semiconductor die attach method to **lead frame** in **semiconductor** packaging - applying thermoplastic or thermoset adhesive to front or back of wafer and patterning adhesive to clear wafer streets and **die** wire bonding pads prior to **die** separation, and attaching adhesive coated **die** to **lead frame** lead fingers

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: CLIFFORD S; FARNWORTH W M; KING J L; MODEN W; SHROCK E A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5286679	A	19940215	US 9333140	A	19930318	199407	B

Priority Applications (No Type Date): US 9333140 A 19930318
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5286679	A		7	H01L-021/60	

Abstract (Basic): US 5286679 A

The **die** attach method involves using bond wires to attach a **die** with multiple bond pads to a **lead frame** with continuous metal lead fingers which extend across the **die** surface to the bond pads. The method involves depositing and patterning either

a thermoplastic or thermosetting adhesive layer on the front of a **semiconductor** wafer prior to singulation of the **dies** from the wafer. The adhesive layer is patterned so that the **die** wire bonding pads, and the streets between **dies**, are free of adhesive material. The adhesive layer may be deposited and patterned using a hot or cold screen printing process, by depositing and photo-patterning a photosensitive adhesive, or using a resist **etch** back method.

During packaging, to attach a **die** to a **lead frame** , the adhesive layer is heated and the lead fingers of the **lead frame** are placed in contact with the **die** under pressure, to bond the lead fingers and the adhesive and attach the lead fingers to the **die**.

USE/ADVANTAGE - Esp. for lead on chip and also lead under chip; chip stacking; adhesive may function as alpha barrier or additional passivation layer.

Dwg.7/9

4/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009064794
WPI Acc No: 1992-192189/**199223**
XRAM Acc No: C92-087971
XRPX Acc No: N92-145128
Multiple **semiconductor** devices within single carrier structure - coupled to leads of **lead-frame** and encapsulated by individual package bodies
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: LIN P T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5114880	A	19920519	US 90538629	A	19900615	199223 B
			US 91680890	A	19910528	

Priority Applications (No Type Date): US 90538629 A 19900615; US 91680890 A 19910528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5114880	A		9	H01L-021/60	Div ex application US 90538629
					Div ex patent US 5036381

Abstract (Basic): US 5114880 A

Fabricating multiple electronic devices within a single carrier structure comprises providing a **lead frame** having **semiconductor die** receiving areas, each of which are surrounded on at least 2 sides by leads having proximal ends near the receiving areas and distal ends away from the receiving area; providing **semiconductor die**; positioning the **semiconductor die** within the receiving areas; electrically coupling the **die** to the proximal ends of the leads of the **leadframe**; providing package bodies which encapsulate each of the **semiconductor die** and portions of the proximal ends of the leads; providing a single carrier structure which encapsulates portions of the distal ends of the leads and encircles the package bodies; allowing individual electrical access to each of the **semiconductor die**.Pref. the package. bodies are excised from the **leadframe**, thereby removing them from the carrier

structure.

USE/ADVANTAGE - Economical and efficient fabrication of multiple electronic devices within a single carrier structure, which protects the leads of the package during handling operations.

Dwg.1/6

7/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008452436
WPI Acc No: 1990-339436/**199045**
Related WPI Acc No: 1990-135849; 1996-474298; 1996-474320; 1996-474333; 1996-474334; 1996-474335; 1996-491041; 1996-491042; 1996-495237; 1997-004959; 1998-318510
XRAM Acc No: C91-155920
XRPX Acc No: N91-277239
Resin-moulded **semiconductor** device - has **lead frame** structure spacing between package base and inner lead is larger than that at chip side
Patent Assignee: HITACHI LTD (HITA); ANJO I (ANJO-I); EGUCHI S (EGUC-I); HASEBE A (HASE-I); HOZOJI H (HOZO-I); ICHITANI M (ICHI-I); KANEDA A (KANE-I); KAWAI S (KAWA-I); KIKUCHI H (KIKU-I); KINJO N (KINJ-I); KITANO M (KITA-I); KOKAKU H (KOKA-I); MATSUMOTO T (MATS-I); MURAKAMI G (MURA-I);

Abstract (Basic): JP 2246125 A
The device includes a cooling mechanism, a high frequency current applying mechanism, and a ring for pressing a substrate having a subject film. The ring is formed of the same material as the subject film at least partly.
USE - Attachment of the ring material to the substrate can be prevented. Yield is improved.
Dwg.1/3
Abstract (Equivalent): US 5612569 A
A **semiconductor** device comprising:
a **semiconductor** chip having a rectangular shape, said **semiconductor** chip including a main surface, a circuit and external terminals formed in said main surface;
an insulating film formed over said main surface and having slits formed therein for defining a first portion and second portions, said first portion of said insulating film extending in a first direction substantially parallel to a longer side of said **semiconductor** chip, said second portions extending towards said longer side of said **semiconductor** chip in a second direction substantially perpendicular to said first direction and said second portions of said insulating film being spaced from each other by said slits in said first direction;
a first lead having a first inner lead portion extending in said first direction and being arranged on said first portion of said insulating film;
second leads spaced from the first lead, each second lead having a second inner lead portion and an outer lead portion, each of said second inner lead portions extending toward said first inner lead portion of said first lead and being arranged, respectively, on each of said second portions of said insulating film;
bonding wires for electrically connecting said external terminals of said **semiconductor** chip with said first and second inner lead portions; and
an encapsulator encapsulating said **semiconductor** chip, said insulating film, said first and second inner lead portions of said first and second leads and said bonding wires.
Dwg.5/78
US 5530286 A
A **semiconductor** device comprising:
a rectangular **semiconductor** chip having a principal surface

with circuit elements and a plurality of external terminals;

a plurality of leads extending over said principal surface, each comprising an inner lead portion and an outer lead portion, said inner lead portion including a first region, a second region and a stepped portion between said first region and said second region;

a plurality of wires for electrically connecting said external terminals with each of said first regions of said inner lead portions; and

a sealing member for sealing said **semiconductor** chip, said inner lead portions and said wires, said sealing member comprising a moulding resin,

wherein a distance between said second region and said principal surface is larger than a distance between said first region and said principal surface.

Dwg.3/78

US 5358904 A

The method comprises the steps of preparing a **semiconductor** chip having a principle surface with circuit elements and numerous external terminals. A **lead frame** has numerous leads each comprising an inner lead portion and an outer lead portion. The inner lead portion includes a first region, a second region and a stepped portion between the first region and the second region. The first and second regions are bonded to the principle surface of the **semiconductor** chip through an insulating film.

Each lead at the first region of the inner leads is connected to each of the external terminals by wire. The chip and the inner lead portions of the leads are moulded in such a way that the chip is supported by the **lead frame**. Part of the inner lead portion extends to overlap with the **semiconductor** chip, the distance between the second region and the principle surface being larger than that between the first region and the principle surface.

ADVANTAGE - High reliability of **semiconductor**. High signal transmission rate. Good heat dissipation. Low parasitic capacitance between leads and chip. High chip productivity.

Dwg.1/77

US 5068712 A

Semiconductor device comprises: a rectangular chip (1) with external terminals and leads; insulator (4) interposed between the chip and inner lead portions (3A); wires (5) connecting the external terminals to first regions of the inner lead portions, the first regions of the inner inner lead portions being nearer the chip surface than second regions to which an outer lead portion (3B) is connected.

USE/ADVANTAGE - Parasitic capacity between chip and leads is reduced to minimise noise and improve signal transmission rate; and device thermal, moulding and moisture-resistance properties are improved. (First major country equivalent to J02246125-A)

Dwg.1/79

7/3,AB/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

008268288

WPI Acc No: 1990-155289/**199020**

XRPX Acc No: N90-120630

Wire bonded **semiconductor** chip - has jumper wires between **lead frame** conductors and parallel conductors which are coupled to terminals by short wires

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: WARD W C
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4916519	A	19900410	US 89358992	A	19890530	199020	B
EP 400324	A	19901205	EP 90107745	A	19900424	199049	
JP 3021047	A	19910129	JP 90137327	A	19900529	199110	
CA 1300761	C	19920512	CA 613496	A	19890927	199225	
EP 400324	A3	19920415	EP 90107745	A	19900424	199328	

Priority Applications (No Type Date): US 89358992 A 19890530
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 400324	A				
Designated States (Regional): DE FR GB IT					
CA 1300761	C			H01L-023/495	

Abstract (Basic): US 4916519 A

A **semiconductor** chip, having a major surface with terminals, is disposed within the encapsulating material. A number of self-supporting, unitary, discrete, and continuous **lead frame** conductors formed of metal sheet stock are positioned at various locations around the chip and cantilevered out of the encapsulating material. Discrete wires can be used to connect the conductors to the terminals.

Excessively long bonding wires are avoided by connecting a selected one of the **lead frame** conductors to a parallel conductor by a jumper wire and connecting the parallel conductor to the desired terminal with a short wire.

ADVANTAGE - Improved mechanical and electrical performance. (7pp Dwg.No. 1/3

7/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008048025
WPI Acc No: 1989-313137/**198943**
Related WPI Acc No: 1989-313138
XRAM Acc No: C91-027795
XRPX Acc No: N91-050842
Process of producing **semiconductor** device - which achieves improved throughput and prodn. yield
Patent Assignee: HITACHI LTD (HITA); HITACHI MFG CO (HITA)
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 1231332	A	19890914	JP 8857520	A	19880311	198943 B
US 4994411	A	19910219	US 89321385	A	19890310	199110
KR 9711649	B1	19970712	KR 892852	A	19890308	199947

Priority Applications (No Type Date): JP 8857520 A 19880311; JP 8857902 A 19880310
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 1231332	A		3		
US 4994411	A		18		
KR 9711649	B1			H01L-021/60	

Abstract (Basic): US 4994411 A
Prodn. of **semiconductor** device comprises providing a **lead frame** having inner leads spaced apart and connected together by a connecting portion; bonding a layer of insulating material to the connecting portion and surrounding portions of inner leads. The connecting portion and a portion of the insualting layer simultaneously are removed to form end portions of the inner leads, which are spaced apart and retained by a remaining portion of insulating layer. A **semiconductor** chip having bonding pads is joined to end portions of leads; connecting bonding pads and inner leads by wires. The device is encapsulated within a resin material wherein a peripheral portion of one face of the **semiconductor** chip partially overlaps faces of the end portions. Pref. the thickness of the end portions of the inner leads and of the connecting portion is smaller than the thickness of the other portions of the **lead frame**.
USE/ADVANTAGE - Process of producing a **semiconductor** device which achieves improved through put and production yield, and is concerned with the joining of a **lead frame** to a **semiconductor** chip followed by encapsulation in a resin. (First major country equivalent to J01231332-A) (18pp Dwg.No.3F/12)

7/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004776625
WPI Acc No: 1986-279966/**198643**
XRAM Acc No: C86-120908
XRPX Acc No: N86-209229
Encapsulated **semiconductor** module - has **lead frame** conductors over and adhered to chip surface

Patent Assignee: IBM CORP (IBMC)
Inventor: PASHBY R P; PHELPS D W; SAMUELSEN S J; WARD W C
Number of Countries: 007 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 198194	A	19861022	EP 86102790	A	19860304	198643	B
JP 61241959	A	19861028	JP 8632066	A	19860218	198649	
CA 1238119	A	19880614				198828	
EP 198194	B	19890614				198924	
DE 3664022	G	19890720				198930	
US 4862245	A	19890829	US 88161319	A	19880219	198944	

Priority Applications (No Type Date): US 85724736 A 19850418; US 86940235 A 19861208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 198194	A	E	16		
Designated States (Regional): DE FR GB IT					
EP 198194	B	E			
Designated States (Regional): DE FR GB IT					

Abstract (Basic): EP 198194 B

A module comprises a chip with terminals, and **lead frame** conductors passing through the encapsulant and connected by wires to the terminals. The conductors partly extend over and are adhesively joined to a substantial part of a chip major surface. The conductors are pref. kinked to mechanically lock the leads within the encapsulant.

Pref. a polyimide film is interposed between the conductors and chip surface and is attached by silicone adhesive to the chip and by epoxy or acrylic adhesive to the conductors. The film is pref. 0.037-0.05 mm thick and the terminals are in rows, one aligned centrally on the surface and such that the conductors over 30-80% of the surface. Av. wire length is pref. less than 0.75 mm.

ADVANTAGE - Provides improved mechanical, electrical and thermal performance. (16pp Dwg.No.4/4

Abstract (Equivalent): EP 198194 B

An encapsulated **semiconductor** module (42) comprising: a **semiconductor** chip (34) having terminals (52) thereon; a plurality of **lead frame** conductors (38) passing through the encapsulating material (46); and wires (58) electrically connecting said conductors to said chip terminals; characterised by: said conductors (38) partly extending over, and being adhesively joined to, a substantial part of a major surface (54) of said chip.

Abstract (Equivalent): US 4862245 A

Encapsulated **semiconductor** module comprises a **semiconductor** chip whose major surface has encapsulated terminals on it. **Lead frame** conductors formed from sheet metal stock extend over and are joined with adhesive in a dielectric relationship to the major surface at spaced positions form the terminals. These conductors extend from the chip and are centilvered out of the encapsulant. The conductors and terminals are connected by individual wires bonded to them.

Pref. there is a dielectric layer between the **lead frame** conductors and the major surface of the chip. This is pref. an alpha barrier and is made of polyimide film. The dielectric layer is attached by adhesive to both the chip and the **lead frame** conductors. The adhesive is pref. an epoxy, acrylic, silicone or polyimide.

ADVANTAGE - The package can be corrected to different chip

terminals, allowing it to be used with different chips. COntamination of the length of the **lead frame** conductors is encapulated.
(9pp)

5. Which of the following amendments to the Constitution does not address or guarantee voting rights?

- 19th Amendment
- 24th Amendment
- 15th Amendment
- **7th Amendment**

20apr04 13:55:35 User267149 Session D1347.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2004/Apr W2
(c) 2004 Institution of Electrical Engineers
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File 6:NTIS 1964-2004/Apr W3
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File 8:Ei Compendex(R) 1970-2004/Apr W2
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File 34:SciSearch(R) Cited Ref Sci 1990-2004/Apr W2
(c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2004/Mar
(c) 2004 ProQuest Info&Learning
File 65:Inside Conferences 1993-2004/Apr W3
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File 94:JICST-EPlus 1985-2004/Apr W1
(c)2004 Japan Science and Tech Corp(JST)
File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Mar
(c) 2004 The HW Wilson Co.
File 144:Pascal 1973-2004/Apr W2
(c) 2004 INIST/CNRS
File 305:Analytical Abstracts 1980-2004/Apr W2
(c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2004/Mar
(c) 2004 DECHEMA
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200425
(c) 2004 Thomson Derwent
*File 350: For more current information, include File 331 in your search. Enter HELP NEWS 331 for details.
File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
(c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2004/Mar
(c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	32	AU=(ESTACIO, M? OR ESTACIO M?)
S2	9	S1 AND SEMICONDUCT?
S3	9	RD (unique items)
S4	5	S3 AND (LEADFRAM? OR LEAD()FRAM?)
S5	4	S2 NOT S4
S6	4	RD (unique items)
S7	23	S1 NOT S2
S8	0	S7 AND ((MULTIPL? OR MULTI OR MANY OR SEVERAL)(3N)LEAD? ?)
S9	0	S7 AND ATTACH?(3N)AREA? ?
S10	3	S7 AND (DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP OR ETCH???????? OR CUT OR TRIM?)
S11	3	RD (unique items)

6/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016009115
WPI Acc No: 2004-166966/200416
Related WPI Acc No: 2003-091779
XRAM Acc No: C04-066139
XRPX Acc No: N04-133073
Manufacture of **semiconductor** die package for e.g., power switching devices, comprises forming carrier, attaching **semiconductor** die to die attach region of carrier, and depositing solder in apertures in solder mask of carrier
Patent Assignee: ESTACIO M C B (ESTA-I); NOQUIL J A (NOQU-I)
Inventor: **ESTACIO M C B**; NOQUIL J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030205798	A1	20031106	US 2001841333	A	20010423	200416 B
			US 2003455511	A	20030604	

Priority Applications (No Type Date): US 2001841333 A 20010423; US 2003455511 A 20030604
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030205798	A1		15	H01L-021/44	Div ex application US 2001841333

Abstract (Basic): US 20030205798 A1
Abstract (Basic):
NOVELTY - A **semiconductor** die package is made by:
(i) forming a carrier (100) having a die attach region, an edge region (106a, 106b), and a solder mask with one or more apertures on the edge region;
(ii) attaching a **semiconductor** die (102) to the die attach region of the carrier; and
(iii) depositing solder in the one or more apertures in the solder mask
USE - For forming a **semiconductor** die package (claimed) for discrete products with high heat dissipation, e.g. power switching devices (e.g., a power metal-oxide-**semiconductor** field effect transistor (MOSFET)) where an electrical connection to a backside of the die (MOSFET drain terminal) is required.
ADVANTAGE - The method increases the strength of the bonds formed between the solder balls and the carrier to improve the reliability of the formed **semiconductor** die package. The package provides for a very low resistance, compact connection between the backside of the die (the drain terminal of the power MOSFET) and a circuit substrate.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a **semiconductor** die package.
Carrier (100)
Semiconductor die (102)
Edge region (106a, 106b)
Solder balls (108-1, 108-2)
First solder mask (110a)
Second solder mask (110b)
pp; 15 DwgNo 1/8

6/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015863120
WPI Acc No: 2004-020951/200402
XRAM Acc No: C04-006579
XRPX Acc No: N04-016059

Semiconductor apparatus comprises gate contact area, gate contact metallization layer, and gate contact passivation layer overlying gate contact metallization layer and having opening(s) exposing portion of gate contact metallization layer

Patent Assignee: BENDAL R E (BEND-I); ESTACIO M C B (ESTA-I); FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: BENDAL R E; **ESTACIO M C B**

Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030189248	A1	20031009	US 2002117890	A	20020408	200402	B
US 6649961	B2	20031118	US 2002117890	A	20020408	200402	

Priority Applications (No Type Date): US 2002117890 A 20020408
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030189248	A1		27	H01L-027/108	
US 6649961	B2			H01L-029/72	

Abstract (Basic): US 20030189248 A1
Abstract (Basic):

NOVELTY - A **semiconductor** apparatus having a robust and reliable metal oxide **semiconductor** field effect transistor (MOSFET) gate external connection, comprises:

(a) gate contact area (51) on first surface of **semiconductor** body and separate from source contact area;

(b) gate contact metallization layer (50) overlying gate contact area; and

(c) gate contact passivation layer overlying gate contact metallization layer and having opening(s) exposing portion of the surface of gate contact metallization layer

DETAILED DESCRIPTION - A **semiconductor** apparatus having a robust and reliable MOSFET gate external connection, comprises:

(a) a **semiconductor** body having a first surface and a second surface;

(b) a source contact area in the first surface of the **semiconductor** body;

(c) a drain contact area on the second surface of the **semiconductor** body;

(d) a gate contact area on the first surface of the **semiconductor** body and separate from the source contact area;

(e) a source contact metallization layer overlying the source contact area;

(f) a gate contact metallization layer overlying the gate contact area;

(g) a source contact passivation layer overlying the source contact metallization layer and having one or more openings exposing a portion of the surface of the source contact metallization layer;

(h) a gate contact passivation layer overlying the gate contact metallization layer and having one or more openings exposing a portion of the surface of the gate contact metallization layer;

(i) a first insulating layer (40) overlying the gate contact passivation layer, overlying one or more exposed area of the source metallization layer and having one or more openings exposing a portion

of the surface of the gate contact metallization layer;

(j) a first conducting metal layer overlying portions of the first insulating layer overlying the one or more exposed area of the source metallization layer and connected to the gate contact metallization layer via the openings in the first insulating layer;

(k) second insulating layer overlying the first conducting metal layer and the first insulating layer and having two or more openings each overlying the source contact metallization layer where each such opening exposes a portion of the surface of the first conducting metal layer;

(l) a second conducting metal layer having two or more zones each overlying and in contact with one exposed portion of the first conducting metal layer, each having an outline of size and shape the same as the exposed portion of the outline of the first conducting metal layerm) a metal plating layer having two or more zones each overlying and in contact with one exposed portion of the second conducting metal layer overlying an exposed portion of the first conducting metal layer, each having an outline of size and shape the same as the exposed portion of the outline of the first conducting metal layer; and

(n) two or more solder bumps each overlying one metal plating layer zone and each having an outline of size and shape the same as the exposed portion of outline of metal plating layer.

INDEPENDENT CLAIM is also included for fabrication of a robust and reliable MOSFET gate external connection on a **semiconductor** apparatus comprising:

(a) coating a first surface of the wafer with a first photosensitive insulating layer;

(b) baking the first photosensitive insulating layer on the wafer;

(c) exposing and developing the first photosensitive layer on the wafer;

(d) sputtering a first conducting metal onto the first insulating layer and the exposed gate and source contact areas;

(e) coating the first conducting metal with a first photoresist coating;

(f) exposing and developing the first photoresist coating to define protected areas for the first conducting metal;

(g) etching the first conducting metal to leave two to more conducting surface pathways of the first conducting metal leading from the gate contact areas to surface areas above the source contact area;

(h) stripping the first photoresist coating;

(i) coating the exposed first photosensitive insulating layer and the exposed first conducting metal with a second photosensitive insulating layer;

(j) baking the second photosensitive insulating layer on the wafer;

(k) exposing and developing the second photosensitive insulating layer to expose the first conducting metal in the surface areas above the source contact area to create two or more exposed gate pad contacts l) sputtering a second conducting metal on the second photosensitive insulating layer and the exposed gate pad contacts;

(m) coating the second conducting metal with a second photoresist coating;

(n) exposing and developing the second photoresist coating to define protected areas of the second conducting metal;

(o) etching the second conducting metal to leave two or more conducting metal areas over the exposed gate pad contacts; and

(p) plating a third conducting metal onto the second conducting metal over the exposed gate pad contacts.

USE - **Semiconductor** apparatus.

ADVANTAGE - The apparatus has a robust and reliable MOSFET gate

external connection. Extension of the underbump metal laterally from the gate contact with gate pad metallization out to two or more gate pads overlying the source pad metallization reduces the risk of delamination of the metallization due to thermal and mechanical stresses in assembly and operation. Use of more than one gate pad further reduces such failure risks. The result is a reliable, durable and economical MOSFET gate contact.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of gate bump and source bump structure.

Gate bump (10)
Source bumps (13)
First insulating layer (40)
Gate contact metallization layer (50)
Gate contact area (51Source metallization (60)
pp; 27 DwgNo 1/34

6/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015634742
WPI Acc No: 2003-696924/200366
XRAM Acc No: C03-191473
XRPX Acc No: N03-556612
Manufacture of **semiconductor** die package used in, e.g. cell phones, involves forming **semiconductor** wafer having **semiconductor** dies defined by scribe lines, forming cavities in the scribe lines, and dicing the wafer along the scribe lines
Patent Assignee: FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: **ESTACIO M C B**
Number of Countries: 102 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030139020	A1	20030724	US 2002351587	P	20020122	200366	B
			US 2003346682	A	20030117		
WO 200363248	A1	20030731	WO 2003US2070	A	20030121	200366	
AU 2003210637	A1	20030902	AU 2003210637	A	20030121	200422	

Priority Applications (No Type Date): US 2002351587 P 20020122; US 2003346682 A 20030117
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030139020	A1		16	H01L-021/301	Provisional application US 2002351587

WO 200363248 A1 E H01L-027/10
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW
AU 2003210637 A1 H01L-027/10 Based on patent WO 200363248

Abstract (Basic): US 20030139020 A1
Abstract (Basic):

NOVELTY - A **semiconductor** die package is made by forming a **semiconductor** wafer comprising **semiconductor** dies (24) defined by scribe lines, forming cavities in the **semiconductor**

wafer in the vicinity of the scribe lines, and dicing the wafer along the scribe lines to separate the **semiconductor** dies comprising a vertical transistor and at least one recess (34) at its edge.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **semiconductor** die package comprising a circuit substrate including a conductive region, a **semiconductor** die comprising a vertical transistor on the circuit substrate, and a solder joint coupling the die and conductive region through the recess. The **semiconductor** die includes an edge and a recess at the edge.

USE - For manufacturing **semiconductor** die package (claimed) used in electronics, e.g. cell phones and lap top computer.

ADVANTAGE - The invention has high on resistance per footprint area, maximizes the drain contacts on the die perimeter through conically-shaped drain connections, and enhances the thermal performance of the **semiconductor** package. The source region of MOSFET in a **semiconductor** die is directly connected to a source contact on a circuit board, thus maximizing the source current to the MOSFET and reducing the on resistance of the MOSFET. The total cross-sectional area for the solder contacts in the **semiconductor** die package is high across the gate, source, and drain. The solder joints can be formed with repeatability and accuracy.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of bumped **semiconductor** dies on chiptrays after dicing.

Semiconductor dies (24)
Solder bumps (32)
Recess (34)
Chiptrays (40)
pp; 16 DwgNo 2b/6

6/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015031262
WPI Acc No: 2003-091779/200308
Related WPI Acc No: 2004-166966
XRAM Acc No: C03-023012
XRPX Acc No: N03-072714

Semiconductor die package manufacturing method e.g for vertical MOSFET, involves forming carrier with die attach region and solder mask with apertures, so as to allow deposition of solder

Patent Assignee: ESTACIO M C B (ESTA-I); NOQUIL J A (NOQU-I); FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: **ESTACIO M C B**; NOQUIL J A

Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020155642	A1	20021024	US 2001841333	A	20010423	200308	B
US 6645791	B2	20031111	US 2001841333	A	20010423	200382	

Priority Applications (No Type Date): US 2001841333 A 20010423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020155642	A1		15	H01L-021/44	
US 6645791	B2			H01L-021/44	

Abstract (Basic): US 20020155642 A1
Abstract (Basic):

NOVELTY - A carrier (100) having die attach and edge regions

(115,106) and a solder mask region (110) having one or more apertures, are formed. A **semiconductor** die (102) is attached to the die attach region of the carrier and solder is deposited in the apertures of the mask.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Carrier; and

(2) **Semiconductor** die package.

USE - For manufacturing **semiconductor** die package (claimed) used for fabricating vertical MOSFET in PCB.

ADVANTAGE - Enables strongly bonded solder contacts to be formed quickly and efficiently in a single process without problems such as mismatch between solder deposits and die package as all the solder deposits are processed in the same way simultaneously.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of the **semiconductor** die package.

Carrier (100)

Semiconductor die (102)

Edge region (106)

Solder mask region (110)

Die attach region (115)

pp; 15 DwgNo 2/8

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? DS

Set     Items   Description
S1         32   AU=(ESTACIO, M? OR ESTACIO M?)
S2          9   S1 AND SEMICONDUCT?
S3          9   RD (unique items)
S4          5   S3 AND (LEADFRAM? OR LEAD()FRAM?)
S5          4   S2 NOT S4
S6          4   RD (unique items)
? TA
>>>No matching display code(s) found in file(s): 65

 6/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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016009115
WPI Acc No: 2004-166966/200416
Related WPI Acc No: 2003-091779
XRAM Acc No: C04-066139
XRPX Acc No: N04-133073
  Manufacture of semiconductor die package for e.g., power switching
  devices, comprises forming carrier, attaching semiconductor die to
  die attach region of carrier, and depositing solder in apertures in
  solder mask of carrier
Patent Assignee: ESTACIO M C B (ESTA-I); NOQUIL J A (NOQU-I)
Inventor: ESTACIO M C B; NOQUIL J A
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No      Kind   Date     Applicat No     Kind   Date      Week
US 20030205798  A1  20031106  US 2001841333    A   20010423  200416  B
                              US 2003455511    A   20030604

Priority Applications (No Type Date): US 2001841333 A 20010423; US
  2003455511 A 20030604
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
US 20030205798 A1    15 H01L-021/44   Div ex application US 2001841333
```

Abstract (Basic): US 20030205798 A1
Abstract (Basic):
NOVELTY - A **semiconductor** die package is made by:
(i) forming a carrier (100) having a die attach region, an edge region (106a, 106b), and a solder mask with one or more apertures on the edge region;
(ii) attaching a **semiconductor** die (102) to the die attach region of the carrier; and
(iii) depositing solder in the one or more apertures in the solder mask
USE - For forming a **semiconductor** die package (claimed) for discrete products with high heat dissipation, e.g. power switching devices (e.g., a power metal-oxide-**semiconductor** field effect transistor (MOSFET)) where an electrical connection to a backside of the die (MOSFET drain terminal) is required.
ADVANTAGE - The method increases the strength of the bonds formed between the solder balls and the carrier to improve the reliability of the formed **semiconductor** die package. The package provides for a very low resistance, compact connection between the backside of the die (the drain terminal of the power MOSFET) and a circuit substrate.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a **semiconductor** die package.
Carrier (100)
Semiconductor die (102)
Edge region (106a, 106b)
Solder balls (108-1, 108-2)
First solder mask (110a)
Second solder mask (110b)
pp; 15 DwgNo 1/8

6/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015863120
WPI Acc No: 2004-020951/200402
XRAM Acc No: C04-006579
XRPX Acc No: N04-016059
Semiconductor apparatus comprises gate contact area, gate contact metallization layer, and gate contact passivation layer overlying gate contact metallization layer and having opening(s) exposing portion of gate contact metallization layer
Patent Assignee: BENDAL R E (BEND-I); ESTACIO M C B (ESTA-I); FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: BENDAL R E; **ESTACIO M C B**
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030189248	A1	20031009	US 2002117890	A	20020408	200402	B
US 6649961	B2	20031118	US 2002117890	A	20020408	200402	

Priority Applications (No Type Date): US 2002117890 A 20020408
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030189248	A1		27	H01L-027/108	
US 6649961	B2			H01L-029/72	

Abstract (Basic): US 20030189248 A1

Abstract (Basic):

NOVELTY - A **semiconductor** apparatus having a robust and reliable metal oxide **semiconductor** field effect transistor (MOSFET) gate external connection, comprises:

(a) gate contact area (51) on first surface of **semiconductor** body and separate from source contact area;

(b) gate contact metallization layer (50) overlying gate contact area; and

(c) gate contact passivation layer overlying gate contact metallization layer and having opening(s) exposing portion of the surface of gate contact metallization layer

DETAILED DESCRIPTION - A **semiconductor** apparatus having a robust and reliable MOSFET gate external connection, comprises:

(a) a **semiconductor** body having a first surface and a second surface;

(b) a source contact area in the first surface of the **semiconductor** body;

(c) a drain contact area on the second surface of the **semiconductor** body;

(d) a gate contact area on the first surface of the **semiconductor** body and separate from the source contact area;

(e) a source contact metallization layer overlying the source contact area;

(f) a gate contact metallization layer overlying the gate contact area;

(g) a source contact passivation layer overlying the source contact metallization layer and having one or more openings exposing a portion of the surface of the source contact metallization layer;

(h) a gate contact passivation layer overlying the gate contact metallization layer and having one or more openings exposing a portion of the surface of the gate contact metallization layer;

(i) a first insulating layer (40) overlying the gate contact passivation layer, overlying one or more exposed area of the source metallization layer and having one or more openings exposing a portion of the surface of the gate contact metallization layer;

(j) a first conducting metal layer overlying portions of the first insulating layer overlying the one or more exposed area of the source metallization layer and connected to the gate contact metallization layer via the openings in the first insulating layer;

(k) second insulating layer overlying the first conducting metal layer and the first insulating layer and having two or more openings each overlying the source contact metallization layer where each such opening exposes a portion of the surface of the first conducting metal layer;

(l) a second conducting metal layer having two or more zones each overlying and in contact with one exposed portion of the first conducting metal layer, each having an outline of size and shape the same as the exposed portion of the outline of the first conducting metal layerm) a metal plating layer having two or more zones each overlying and in contact with one exposed portion of the second conducting metal layer overlying an exposed portion of the first conducting metal layer, each having an outline of size and shape the same as the exposed portion of the outline of the first conducting metal layer; and

(n) two or more solder bumps each overlying one metal plating layer zone and each having an outline of size and shape the same as the exposed portion of outline of metal plating layer.

INDEPENDENT CLAIM is also included for fabrication of a robust and reliable MOSFET gate external connection on a **semiconductor** apparatus comprising:

(a) coating a first surface of the wafer with a first photosensitive insulating layer;
(b) baking the first photosensitive insulating layer on the wafer;
(c) exposing and developing the first photosensitive layer on the wafer;
(d) sputtering a first conducting metal onto the first insulating layer and the exposed gate and source contact areas;
(e) coating the first conducting metal with a first photoresist coating;
(f) exposing and developing the first photoresist coating to define protected areas for the first conducting metal;
(g) etching the first conducting metal to leave two to more conducting surface pathways of the first conducting metal leading from the gate contact areas to surface areas above the source contact area;
(h) stripping the first photoresist coating;
(i) coating the exposed first photosensitive insulating layer and the exposed first conducting metal with a second photosensitive insulating layer;
(j) baking the second photosensitive insulating layer on the wafer;
(k) exposing and developing the second photosensitive insulating layer to expose the first conducting metal in the surface areas above the source contact area to create two or more exposed gate pad contacts
l) sputtering a second conducting metal on the second photosensitive insulating layer and the exposed gate pad contacts;
(m) coating the second conducting metal with a second photoresist coating;
(n) exposing and developing the second photoresist coating to define protected areas of the second conducting metal;
(o) etching the second conducting metal to leave two or more conducting metal areas over the exposed gate pad contacts; and
(p) plating a third conducting metal onto the second conducting metal over the exposed gate pad contacts.
USE - **Semiconductor** apparatus.
ADVANTAGE - The apparatus has a robust and reliable MOSFET gate external connection. Extension of the underbump metal laterally from the gate contact with gate pad metallization out to two or more gate pads overlying the source pad metallization reduces the risk of delamination of the metallization due to thermal and mechanical stresses in assembly and operation. Use of more than one gate pad further reduces such failure risks. The result is a reliable, durable and economical MOSFET gate contact.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of gate bump and source bump structure.
Gate bump (10)
Source bumps (13)
First insulating layer (40)
Gate contact metallization layer (50)
Gate contact area (51Source metallization (60)
pp; 27 DwgNo 1/34

6/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015634742
WPI Acc No: 2003-696924/200366
XRAM Acc No: C03-191473
XRPX Acc No: N03-556612
Manufacture of **semiconductor** die package used in, e.g. cell phones,

involves forming **semiconductor** wafer having **semiconductor** dies defined by scribe lines, forming cavities in the scribe lines, and dicing the wafer along the scribe lines

Patent Assignee: FAIRCHILD SEMICONDUCTOR CORP (FAIH)

Inventor: **ESTACIO M C B**

Number of Countries: 102 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030139020	A1	20030724	US 2002351587	P	20020122	200366	B
			US 2003346682	A	20030117		
WO 200363248	A1	20030731	WO 2003US2070	A	20030121	200366	
AU 2003210637	A1	20030902	AU 2003210637	A	20030121	200422	

Priority Applications (No Type Date): US 2002351587 P 20020122; US 2003346682 A 20030117

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030139020	A1		16	H01L-021/301	Provisional application US 2002351587
WO 200363248	A1	E		H01L-027/10	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

AU 2003210637 A1 H01L-027/10 Based on patent WO 200363248

Abstract (Basic): US 20030139020 A1

Abstract (Basic):

NOVELTY - A **semiconductor** die package is made by forming a **semiconductor** wafer comprising **semiconductor** dies (24) defined by scribe lines, forming cavities in the **semiconductor** wafer in the vicinity of the scribe lines, and dicing the wafer along the scribe lines to separate the **semiconductor** dies comprising a vertical transistor and at least one recess (34) at its edge.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **semiconductor** die package comprising a circuit substrate including a conductive region, a **semiconductor** die comprising a vertical transistor on the circuit substrate, and a solder joint coupling the die and conductive region through the recess. The **semiconductor** die includes an edge and a recess at the edge.

USE - For manufacturing **semiconductor** die package (claimed) used in electronics, e.g. cell phones and lap top computer.

ADVANTAGE - The invention has high on resistance per footprint area, maximizes the drain contacts on the die perimeter through conically-shaped drain connections, and enhances the thermal performance of the **semiconductor** package. The source region of MOSFET in a **semiconductor** die is directly connected to a source contact on a circuit board, thus maximizing the source current to the MOSFET and reducing the on resistance of the MOSFET. The total cross-sectional area for the solder contacts in the **semiconductor** die package is high across the gate, source, and drain. The solder joints can be formed with repeatability and accuracy.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of bumped **semiconductor** dies on chiptrays after dicing.

Semiconductor dies (24)

Solder bumps (32)

Recess (34)

Chiptrays (40)
pp; 16 DwgNo 2b/6

6/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015031262
WPI Acc No: 2003-091779/200308
Related WPI Acc No: 2004-166966
XRAM Acc No: C03-023012
XRPX Acc No: N03-072714
Semiconductor die package manufacturing method e.g for vertical MOSFET, involves forming carrier with die attach region and solder mask with apertures, so as to allow deposition of solder
Patent Assignee: ESTACIO M C B (ESTA-I); NOQUIL J A (NOQU-I); FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: **ESTACIO M C B**; NOQUIL J A
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020155642	A1	20021024	US 2001841333	A	20010423	200308 B
US 6645791	B2	20031111	US 2001841333	A	20010423	200382

Priority Applications (No Type Date): US 2001841333 A 20010423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020155642	A1		15	H01L-021/44	
US 6645791	B2			H01L-021/44	

Abstract (Basic): US 20020155642 A1
Abstract (Basic):
NOVELTY - A carrier (100) having die attach and edge regions (115,106) and a solder mask region (110) having one or more apertures, are formed. A **semiconductor** die (102) is attached to the die attach region of the carrier and solder is deposited in the apertures of the mask.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Carrier; and
(2) **Semiconductor** die package.
USE - For manufacturing **semiconductor** die package (claimed) used for fabricating vertical MOSFET in PCB.
ADVANTAGE - Enables strongly bonded solder contacts to be formed quickly and efficiently in a single process without problems such as mismatch between solder deposits and die package as all the solder deposits are processed in the same way simultaneously.
DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of the **semiconductor** die package.
Carrier (100)
Semiconductor die (102)
Edge region (106)
Solder mask region (110)
Die attach region (115)
pp; 15 DwgNo 2/8

11/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014397442
WPI Acc No: 2002-218145/200228
XRPX Acc No: N02-167196
Multiple chip component with wireless packing has **dies** or chip elements with bumps on lower line frames, upper line frames coupled to **dies**, connecting rails interconnected in pairs
Patent Assignee: FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: BAJE G S; **ESTACIO M C B**; GESTOLE M A; LEDON O M; MEPIEZA S; QUINONES M C Y
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10102197	A1	20010816	DE 1002197	A	20010118	200228	B
JP 2001257302	A	20010921	JP 200110825	A	20010118	200228	
TW 529138	A	20030421	TW 2001100846	A	20010115	200373	

Priority Applications (No Type Date): US 2000487969 A 20000118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10102197	A1		17	H01L-023/495	
JP 2001257302	A		11	H01L-023/48	
TW 529138	A			H01L-023/28	

Abstract (Basic): DE 10102197 A1
Abstract (Basic):
NOVELTY - The component has lower line frames (11), **dies** or chip elements with bumps on lower line frames with source and gate solder bump arrays, upper line frames (13), each coupled to a **die** with bumps and containing lines and four rails interconnected in pairs with sides connected to the frames. Each lower frame has lines with drain connections coupled to **dies** with bumps. Each upper frame has lines coupled to gate and source connections on a **die**.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: a method of manufacturing a chip component, especially an improved method of packing several DMOS components.
USE - Multiple chip component.
ADVANTAGE - Wireless packing of chip components is achieved to enable high volume manufacture in a production environment.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic perspective representation of upper and lower line frames
lower line frame (11)
upper line frame (13)
lines (21,25)
pp; 17 DwgNo 4/8

11/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07124273
FLIP-CLIP ATTACH AND COPPER CLIP ATTACH ON MOSFET DEVICE

PUB. NO.: 2001-351941 [JP 2001351941 A]
PUBLISHED: December 21, 2001 (20011221)
INVENTOR(s): **ESTACIO MARIA CHRISTINA B**

KUINONESU MARIA CLEMENS Y
APPLICANT(s): FAIRCHILD SEMICONDUCTOR CORP
APPL. NO.: 2001-114665 [JP 2001114665]
FILED: April 12, 2001 (20010412)
PRIORITY: 00 548946 [US 2000548946], US (United States of America), April 13, 2000 (20000413)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of manufacturing a chip which includes direct mounted the chip devices and **dies** with bumps on a lead frame and the attachment of a set of leads to the **dies** with bumps, using clips.

SOLUTION: The method of manufacturing a chip includes a step of providing the **dies** with bumps having a plurality of solder humps, a step of providing the lead frame having source and gate connections, and a step arranging the **dies** with bumps on the lead frame, so that the solder bumps come into contact with the source and gate connections. The method also includes a step of attaching copper clips to the rear surfaces of the **dies** with bumps using solder paste, so that the clips come into contact with the drain regions and lead rails of the **dies** with bumps and a step of reflowing the solder paste and solder bumps.

11/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

07029668
IMPROVED METHOD OF MANUFACTURING CHIP DEVICE

PUB. NO.: 2001-257302 [JP 2001257302 A]
PUBLISHED: September 21, 2001 (20010921)
INVENTOR(s): QUINONES MARIA CLEMENS Y
BAJE GILMORE S
ESTACIO MARIA CHRISTINA B
GESTOLE MARVIN R
LEDON OLIVER M
MEPIEZA SANTOS
APPLICANT(s): FAIRCHILD SEMICONDUCTOR CORP
APPL. NO.: 2001-010825 [JP 200110825]
FILED: January 18, 2001 (20010118)
PRIORITY: 00 487969 [US 2000487969], US (United States of America), January 18, 2000 (20000118)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method and equipment for manufacturing a 'wireless' package of a chip device, in a mass-production environment.
SOLUTION: A plurality of chip devices comprise a plurality of bottom lead frames, a plurality of bumped **dies**, a plurality of upper lead frames, and four rails. The first rail is connected to each of first side faces of the upper lead frames, the second rail is connected to each of second side faces of the upper lead frames, the third rail is connected to each of first side faces of the bottom lead frames, and the fourth rail is connected to each of second side faces of the bottom lead frames.